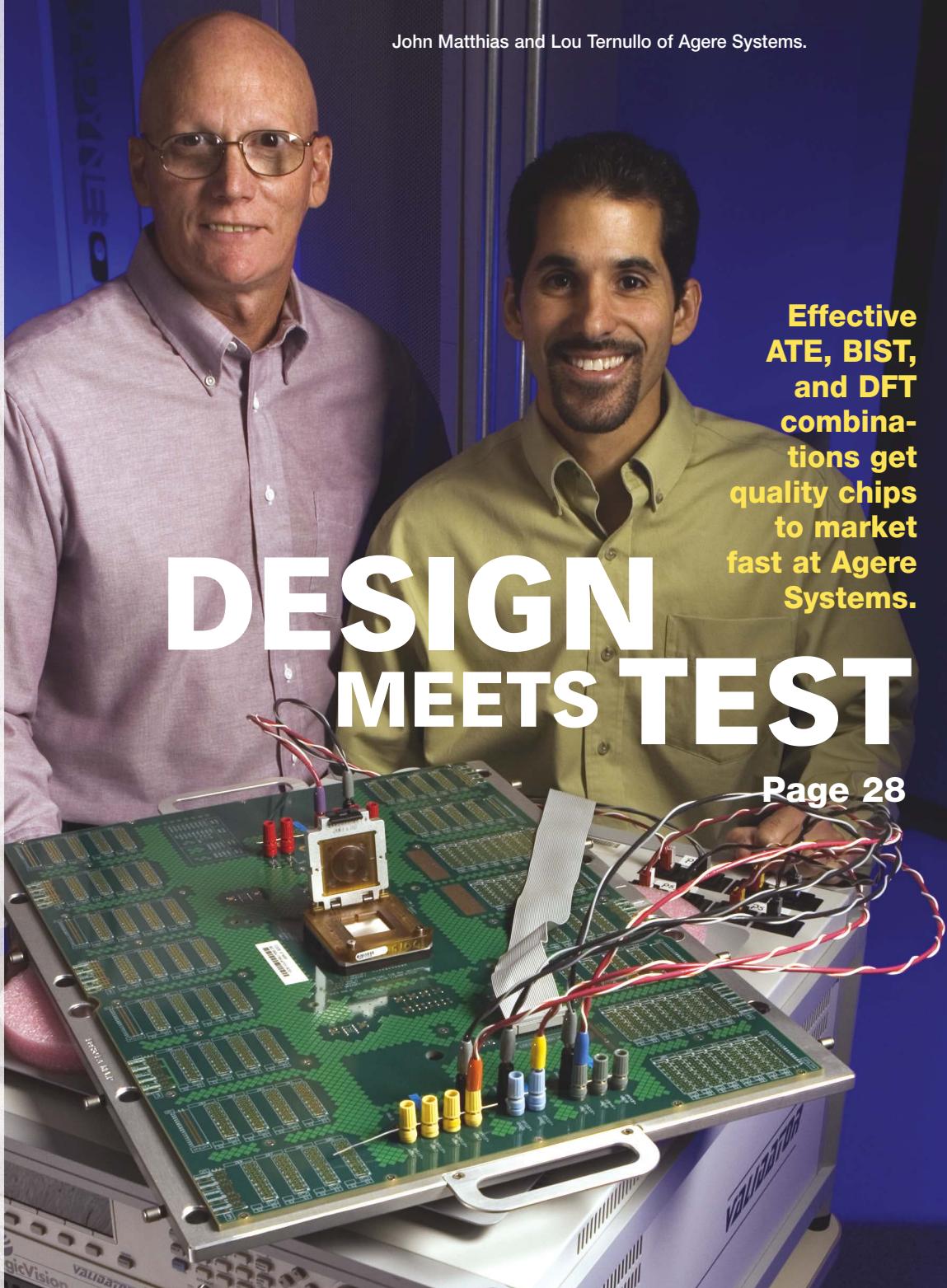


test & MEASUREMENT WORLD®

THE MAGAZINE FOR QUALITY IN ELECTRONICS

PROJECT PROFILE**Chamber verifies quiet designs****27****DESIGN FOR TEST****IEEE 1149 expands differentially****39****INSPECTION****X-ray systems sharpen images****43****TECH TRENDS****Choose your domain****19****TECH TRENDS****How much test is enough?****21**

John Matthias and Lou Ternullo of Agere Systems.



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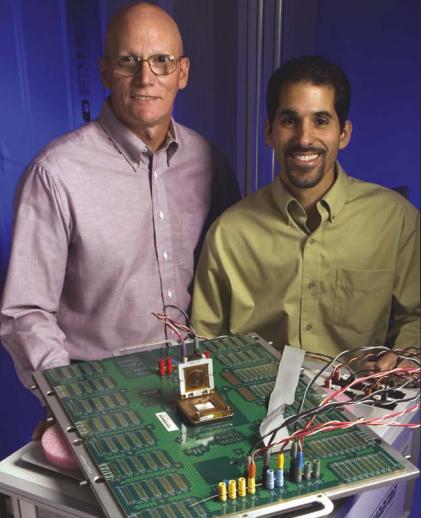


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COVER BY: ED WHEELER

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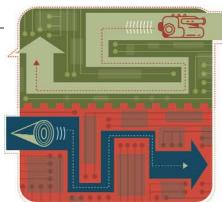
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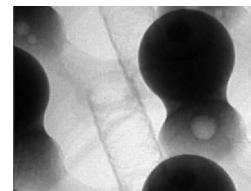


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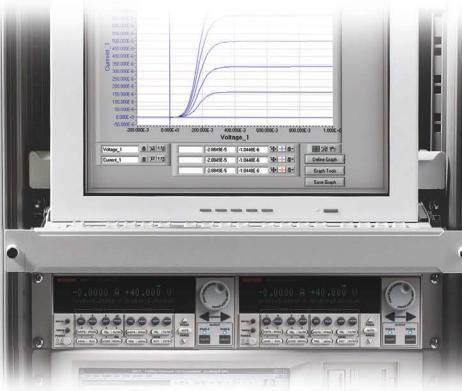
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Best in test: people and products

Last month, we highlighted six outstanding test-engineering professionals as the kickoff to our annual awards programs. Our editors selected these six nominees from among suggestions sent in by *Test & Measurement World* readers. Now, the ball is back in your court. Please review each candidate's qualifications. Among the highlights:

- Ken Coleman configures hardware and software for testing ink-jet print heads at Lexmark, and, when at IBM, he earned patents for keyboard designs and has served on a committee to address repetitive-stress injuries.

**RICK NELSON, CHIEF EDITOR**

• Michael Freeman develops custom automated test hardware and software at Broadcom, has authored many technical papers, and still finds the time to serve as president of his local chapter of the American Society of Test Engineers.

• Georgia Harris of the National Institute of Standards and Technology oversees the accreditation programs for 50 state laboratories. In addition, she has spearheaded metrology quality and training programs and has established proficiency tests for metrologists.

• Herman Chu has set up thermal engineering labs for several companies, including Cisco Systems, where he works now. Intent on finding creative solutions to ever-increasing power consumption, he has authored many papers and chaired packaging workshops.

• John Kauffman of Rockwell Collins developed a data-management system to streamline tests related to the military's Joint Tactical Radio System. A stint in the Marines as a metrology-services coordinator taught him the value of cooperation among government, contractor, and instrument-vendor personnel.

• Zafer Boz emigrated from Turkey to the UK, where he develops test software that lets his colleagues at STMicroelectronics focus on test, not code compilation. He's completing an MSEE degree and hopes to build a career managing test projects.

Please read more about these nominees in our September issue or at www.tmworld.com/teoty. Then, cast your vote by November 1. We realize there are many other worthy candidates out there, so be prepared to nominate them for next year's award.

In addition to our Test Engineer of the Year award, we are also inviting test-equipment vendors to nominate their products and services for our annual Best in Test awards, which honor products introduced in 2005 (see www.tmworld.com/awards for more).

From among the Best in Test nominations we receive, editors will select 12 to feature in our double December 2005/January 2006 issue. Then, we will ask for your help again—to cast your vote for the Test Product of the Year, to be presented at our award ceremony held in February 2006. T&MW

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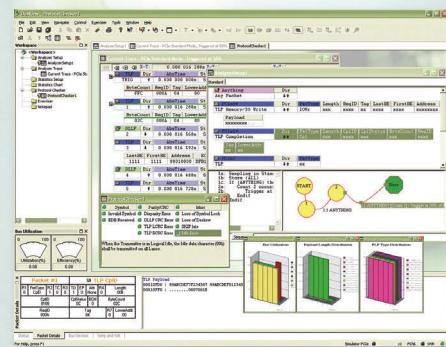
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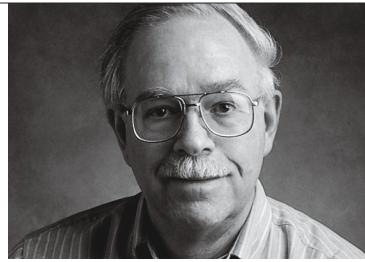
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Logistics nightmares

My cranky 1960s-vintage spectrum analyzer nears the end of its service life, and announcement of a \$500, 150-kHz to 500-MHz spectrum analyzer with a CRT display piqued my curiosity. But the analyzer's Chinese origin poses potentially troublesome logistics issues. Its spare parts and tech support originate from half a world away.

Instruments aside, I usually think about logistics only when I shop for groceries. That changed when Hurricane Katrina slammed into the Gulf Coast, destroying parts of New Orleans and severely impacting gas and oil production from the Gulf. In the storm's wake, gas prices surged upward and spot shortages appeared. Logistics SNAFUs impacted evacuation of survivors and delivery of desperately needed aid. Survivors found it difficult or impossible to obtain cash or gain access to financial records and bank accounts. One federal relief agency offered to mail survivors' relief checks to homes that no

longer exist—a logistics challenge in its own right!

Our globalized electronics industry relies heavily on just-in-time (JIT) manufacturing. Reliance on offshore labor and component sources have lengthened the supply chain and emphasized sole sources.

While a small fire in a

supplier's factory can significantly affect a single product, a major earthquake in Taiwan could cripple production of many components, creating a cascade of shutdowns and layoffs in businesses that depend on uninterrupted JIT deliveries.

Potential logistics problems extend beyond parts and petroleum. Many companies have moved data processing and technical support services to politically and socially unstable areas offering low-cost labor. In recent years, India, Pakistan, and China have narrowly avoided war, but a major conflict between India and Pakistan would cripple both nations. With overseas contractors' operations shut down or destroyed, domestic manufacturers and financial institutions couldn't offer support and services. Redundant stateside backup facilities cost money to maintain and would thus eliminate globalization's financial benefits.

I'm getting an uneasy feeling that our electronics-intensive civilization is tap dancing its way toward disaster along an increasingly narrow and brittle supply chain. Will someone please tell me otherwise? T&MW



FOR MORE INFORMATION

To learn more about an inexpensive RF spectrum analyzer, go to:

www.attenu.com.cn

The basic instrument carries a nominal price tag of \$500, which averages out to \$1 per MHz, a modest price indeed for a spectrum analyzer. It isn't manufactured here in the US—it's a product of Atten Electronics Co., Shenzhen, People's Republic of China. The usual disclaimers apply: I haven't reviewed or otherwise evaluated this instrument and have no interest, financial or otherwise, in the manufacturer or the product.

To learn more about globalization's effects and where the world's economy may be headed, read:

The World Is Flat: A Brief History of the Twenty-First Century, by Thomas L. Friedman, Farrar, Straus and Giroux, 2005. ISBN 0-374-29288-4.

For an exploration of globalization and its potential logistics perils, consider reading:

End of the Line: The Rise and Coming Fall of the Global Corporation, by Barry C. Lynn, Doubleday division of Random House, 2005. ISBN 0-385-51024-1.

This interesting blog site offers an assortment of opinions and insights into globalization and its effects:

www.enterblog.com/index.html.

For a brief article summarizing issues posed by globalization's increasing stress on logistics processes, go to:

www.purchasing.com/article/CA624893

For a more extensive analysis of globalization's effects on world economies, and a discussion of why Friedman's "flat world" theory may not exactly reflect reality, read:

"The World Is Spiky: Globalization has changed the economic playing field, but hasn't leveled it", by Richard Florida, *Atlantic Monthly*, October 2005, pp. 48-51.



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Harbor Electronics joins Everett Charles Technologies

Executives and shareholders of Harbor Electronics, a manufacturer of PCBs for semiconductor test applications, announced a decision to join Everett Charles Technologies (ECT). Harbor VP Tim McNulty (pictured) has been appointed president of ECT's Semiconductor Test Group (STG) and will be responsible for the existing STG-MN (St. Paul) and STG-AZ (Tempe) operations, in addition to Harbor Electronics.

Pat Flynn, president of ECT, commented, "Harbor has established a leading position in their market, and we are convinced this trend will continue. Harbor's advanced PCB manufacturing capabilities and capacity complement our existing test socket, performance board, and IC handler product lines and augment STG's leadership position in this segment of the semiconductor test industry. This transaction serves as another indicator to our global customer base that STG is committed to providing local support, wherever they do business, with world-class products and services." www.ectinfo.com.



Electro Rent opens European operation

Electro Rent, a test-and-measurement and computer-equipment rental company with operations in North America and China, has established Electro Rent Europe. ER Europe was scheduled to commence operations at the end of September.

As part of its plans, ER has acquired the operations of Everest ES, a Belgium equipment rental, sales, and leasing business, which has been operating in an alliance with Electro Rent for several years. David Saeys, the owner of Everest, will become the GM of ER Europe.

"We are very excited about establishing a local presence to provide quality service at competitive prices in the European market," commented Dan Greenberg, Electro Rent chairman and CEO. "We intend to build a significant market presence and provide European technology companies with access to one world's largest inventories of test and measurement and computer equipment." www.electorent.com.

VIA employs Tektronix instruments

Tektronix reports that Taiwan-based VIA Technologies has selected digital systems analysis tools from Tektronix for developing digital products based on serial data standards such as second-generation PCI-Express and SATA III. To perform design validation and interoperability and compliance testing on its products, VIA has selected the TLA7012

and TLA7016 logic analyzers, the 12-GHz TDS 6124C oscilloscope, and the 15-GHz TDS 6154C real-time oscilloscope. TLA7000 series logic analyzers include the iLink tool set, which integrates the logic analyzer with an oscilloscope to speed the debugging of multiple signals.

"High-speed serial buses such as second-generation PCI Express and SATA III present new challenges when making

design and compliance measurements," said Chewei Lin, VP of product marketing at VIA Technologies. "The combination of TLA7000 logic analyzers and TDS6000 oscilloscopes from Tektronix supports our measurement needs at each stage of design, validation, compliance, and debug, and will enable our engineers to test high-speed serial designs with total confidence." www.tektronix.com; www.via.com.tw.

Scopes handle 100-MHz applications

Agilent Technologies has put the features of its DSO/MSO 6000 series oscilloscopes into four 100-MHz models. Like the series' 300-MHz, 500-MHz, and 1-GHz models, the 100-MHz version is available in two-channel and four-channel units with and without

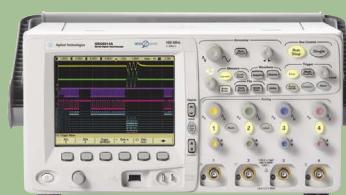
16 logic inputs. Designed for embedded-system developers who need to look at microcontroller I/O signals, these mixed-signal scopes let you trigger an acquisition on a 16-bit digital pattern and on a set of analog conditions such as voltage

level. Specific signal triggers include USB, I²C, and CAN serial buses as well as numerous TV-signal triggers.

Each of the four 100-MHz models samples signals at 2 Gsamples/s and can store up to 1 Msample over two channels. Four-channel models store 500 ksamples on each pair of channels when running three or four channels. Upgrades boost waveform memory from 1 Msample to either 2 Msamples or 8 Msamples. The deep memory lets the scopes maintain full sample rate at any timebase setting. All models have a screen update rate of 100,000 waveforms/s and include IEEE 488, Ethernet, and USB ports.

The four models range in price from \$4595 for a two-channel unit to \$7595 for a four-channel unit with 16 logic inputs. Agilent Technologies, WWW.AGILENT.COM/FIND/SCOPE-NEW.

EDITORS' CHOICE



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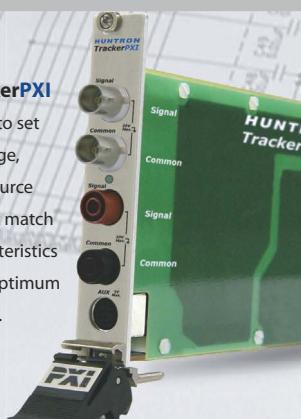
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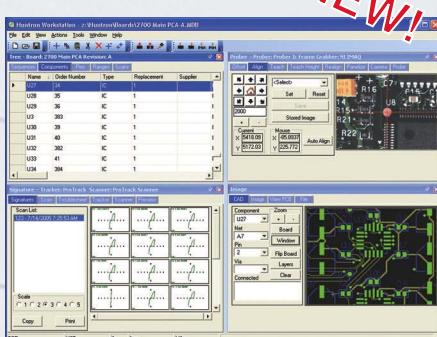
enables the user to set the applied voltage, frequency and source resistance to best match the circuit characteristics and display the optimum Tracker signature.



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NEW!



HUNTRON
Access Explore Discover

For more information, call or click, 800-426-9265 or www.huntron.com

NEWSBRIEFS

CIVA simulation tool available in North America

Magsoft has announced an agreement with Commissariat à l'Energie Atomique (CEA) covering the sale, distribution, and support of the CEA's simulation software—CIVA release 7.1—in North America. CIVA, a computer-aided-engineering (CAE) simulation tool, solves problems for a variety of application and device configurations concerning nondestructive evaluation. It simulates the design of nondestructive sensor components and is currently available for both eddy-current and ultrasonic methods of detection.

CIVA combines a graphical user interface with semi-analytical methods to let the user define a problem, solve it, and review the results. The user can explore the nature of a transmission signal that produces the optimal reflections for determining whether a flaw exists. CIVA is suited for sensor designs intended to detect flaws for the aircraft and aerospace industries, Magsoft reports.

"CIVA is exciting new technology, and we are proud to be the conduit for

CALENDAR

International Test Conference (ITC), November 8–10, Austin, TX. Sponsored by IEEE. www.itctestweek.org.

Vision 2005, November 8–10, Stuttgart, Germany. Sponsored by Messe Stuttgart. www.vision-messe.de.

Productronica, November 15–18, Munich, Germany. Sponsored by Messe Muenchen. www.global-electronics.net/id/21310.

To learn about other conferences, courses, and calls for papers, visit www.tmworld.com/events.

its entry into North America," said Shep Salon, president of Magsoft. "This technology can really make an impact on a variety of industries and marketplaces, and it can help to make the world a cleaner, safer place, which benefits us all." www.magsoft-flux.com.

Smart cameras get remote heads

Matrox Imaging has announced remote-head versions of its Iris P-Series family of programmable smart cameras, which combine image-sensing and processing hardware with a software API for image analysis. The new cameras employ a two-piece design in which a standard Camera Link cable connects a remote head to

a processor unit. The compact remote head is designed to fit small spaces and to offer flexibility for deployment in equipment destined for automotive, electronics, robotics, and other applications.

An Intel Ultra Low Power (ULP) Celeron embedded processor runs the Windows

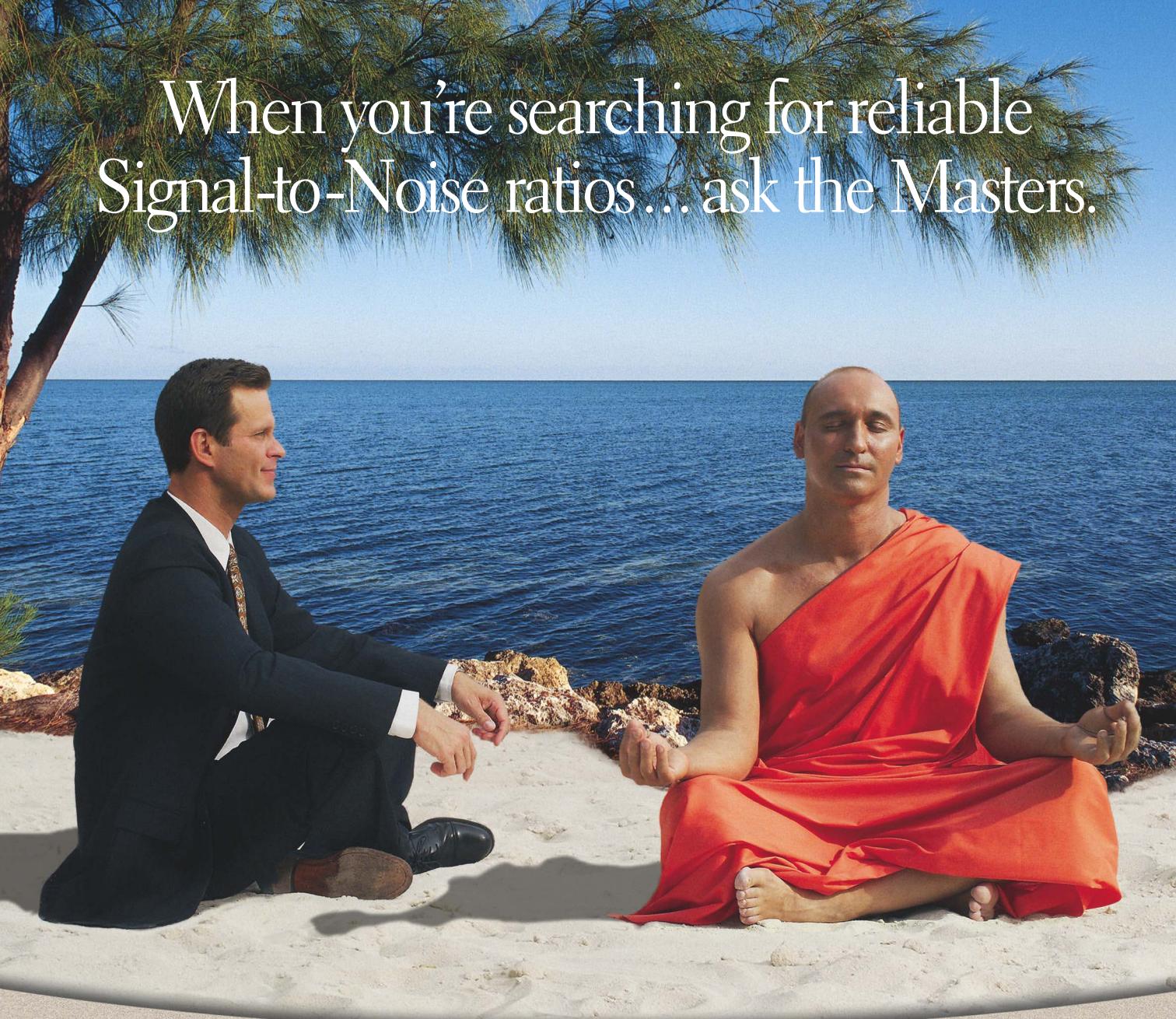
CE .NET real-time operating system in each processor unit, which is programmable using Microsoft's embedded Visual C++ language. OEMs and integrators can develop their own image capture, processing, analysis, display, and archiving applications with the Matrox Imaging Library (MIL) software; those applications will run directly on Matrox Iris P-Series units. Onboard flash and SDRAM memory store the operating system, MIL, and a custom machine-vision application. Data communications can take place over Ethernet and RS-232 ports.

Base price: \$2495. Matrox Imaging, WWW.MATROX.COM/IMAGING.

EDITORS' CHOICE



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EMC engineers gather on Lake Michigan

>>> 2005 IEEE Symposium on Electromagnetic Compatibility, August 8–12, Chicago, IL, www.emcs.org.

This year's IEEE EMC Symposium featured more than 200 technical papers, forums, technical sessions, and tutorials. In the keynote address, "Advanced Wireless Systems, Seamless Mobility, and EMC," Gary Graube of Motorola's Government and Enterprise Mobility Solutions Business focused on "The device formerly called a cell phone" that now takes photos, views Web pages, plays music, and connects to any network. He discussed the EMC challenges in today's ever-shrinking consumer products.

The technical program featured sessions on EMC measurements, including papers on EMI measurements above 1 GHz. Andrew Marvin and Yong Cui from the University of York experimented with an enclosure that contained an EMI-radiating board. They found that the position of the board inside the enclosure greatly affected emissions radiated outside the enclosure. Alexander Kriz of ARC Seibersdorf Research followed with "Validating Anechoic Chambers Above 1 GHz Using a Reciprocal Site VSWR Technique." He pointed out that EMI antennas take on different characteristics above 1 GHz.

When discussing experiments on circuit-to-circuit interference, Silent Solution's Randall Vaughn showed how replacing components in a circuit can change its EMC characteristics. Consultant Doug Smith demonstrated how a common ground between two chassis created interference from one chassis to the other.

In "Shielded Enclosure Accuracy Improvements for MIL-STD-461E Radiated Emissions Measurements," Andy Wang and David Wartenkin from General Dynamic Canada explained how they discovered inconsistencies in measurements made in shielded enclosures that complied with the standard. Wartenkin modeled the chamber with software, and his results were consistent with the measurements in the chamber.

Other demonstrations included antenna pattern measurements by Dr. Michael Fogelle of ETS-Lindgren. He showed how the radiating patterns of EMI antennas change at frequencies above 1 GHz. Tim Lusha and Josh Bakk of DLS Electronic Systems demonstrated how to verify MIL-STD measurements. They showed two test jigs for measuring voltage and current using continuous wave and pulsed RF signals.

On the exhibit floor, **AR Worldwide** (www.ar-worldwide.com) entered the market

for EMI receivers with the introduction of the CER2012. The receiver uses a modular design containing plug-ins with several frequency ranges that expand bandwidth from 12 GHz to 90 GHz. **Haefely Technology** (www.haefelyemc.com) introduced the ECompact4 immunity tester, which performs tests such as surges, electrical fast transients, dips and interrupts, and AC/surge magnetic fields.

Credence Technologies (www.credencetech.com) introduced an active dipole EMI antenna with a built-in equalizing preamp that increases its sensitivity at lower frequencies, making it comparable to a conventional log-periodic antenna. **HV Technologies** (www.hvtechnologies.com) displayed a lightning simulator for aircraft testing to the DO-160D military standard.

ETS-Lindgren (www.ets-lindgren.com) demonstrated its new LaserPro line of E-field probes. These probes don't require batteries, which gives them an advantage in long tests (typical batteries last 8–10 hrs). The probes get their power from a fiber-optic cable that carries infrared light from a light source. **X-EMI** (www.x-emi.com) introduced an IC that reduces EMI emissions in serial communications buses. **T&MW**



Tim Lusha explained how to verify calibrations for MIL-STD EMI measurements.

DSPs get LabView support; PXI Express spec set

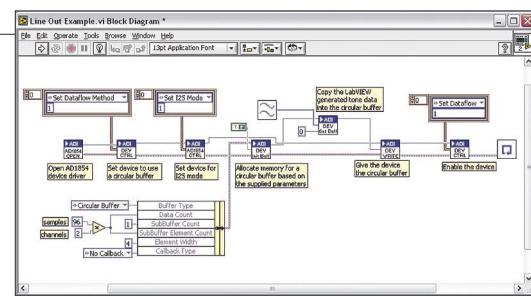
>>> NIWeek 2005, August 16–18, Austin, TX, www.niweek.com.

Analog Devices (www.analog.com) teamed up with **National Instruments** (www.ni.com) to announce the availability of the public beta version of the NI LabView Embedded Module for ADI Blackfin processors. The software module provides design engineers with early access to a seamless, graphical dataflow development approach that directly targets Blackfin processors. The companies also announced that NI can integrate Analog Devices' ADIsimADC analog-to-digital converter modeling software with NI SignalExpress to provide engineers with a virtual benchtop for device simulation and evaluation.

Goepel electronic (www.goepel.com) introduced a family of PXI-based boundary-scan controllers for its Scanflex boundary-scan hardware. Like the company's PCI-based and USB 2.0-based controllers introduced earlier this year, the PXI modules are available in three performance classes that differ in the upper TCK frequency limit (max-

imum of 20, 50, or 80 MHz, respectively) as well as in the level of implementation of the vendor's enhanced SPACE II chip set for high-performance scan operations. The new SFX/PXI1149 boundary-scan controllers support all trigger features provided by the PXI specification.

National Instruments also demonstrated its NI MXI-Express kits for PCI Express control of PXI and CompactPCI systems. Based on PCI Express, MXI-Express delivers real-world sustained bandwidth of up to 110 Mbytes/s to PXI systems. The company



A new LabView embedded module provides design engineers with a graphical dataflow development approach that targets Analog Devices' Blackfin processors.

Courtesy of National Instruments.

also highlighted what it calls the industry's first PC-based multifunction data-acquisition (DAQ) devices for PCI Express. The NI PCIe-6251 and NI PCIe-6259 DAQ devices combine the high-performance PCI Express bus with technology advancements of National Instruments' M Series DAQ to offer engineers and scientists fast analog and digital I/O with the dedicated per-slot bandwidth of PCI Express. The new devices feature up to 32 analog channels with 16-bit, 1.25-Msample/s sampling speed and 10-MHz digital I/O on up to 32 lines.

Concurrently with NIWeek, the **PXI Systems Alliance** (www.pxisa.org) held a press conference to officially announce its PXI Express specification, which integrates PCI Express and CompactPCI Express technology into the PXI instrument-interface standard. With PXI Express, engineers and scientists can achieve bandwidths up to 6 Gbps per system, representing a 45-fold improvement when compared to traditional PXI systems.

Although PXI Express-compliant products won't ship until early next year, several manufacturers were on hand at the press conference to demonstrate their support for the new spec: **Aeroflex** (www.aeroflex.com), **Ascor** (www.ascor.com), **B&B Technologies** (www.bbtechno.com), **Conduant** (www.conduant.com), **Elma Bus-tronic** (www.bustronic.com), **Geotest** (www.geotestinc.com), Goepel electronic, and **Ztec** (www.ztec-inc.com), as well as NI.

In addition, chip makers **Intel** (www.intel.com) and **Xilinx** (www.xilinx.com) were on hand to emphasize their efforts to produce the silicon engines that could drive the emerging PXI Express applications. **T&MW**



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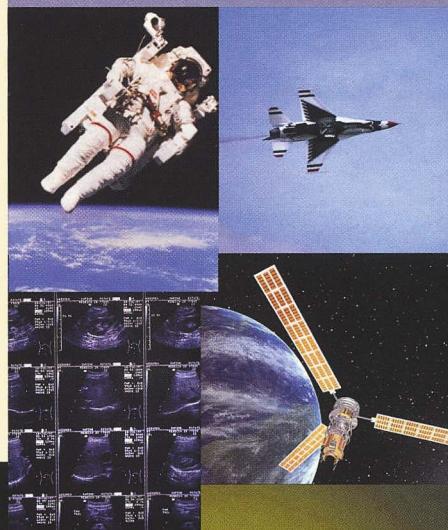


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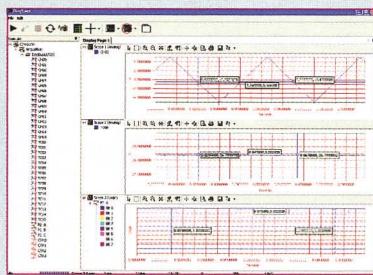


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Choose your domain

Time and frequency are closely related. In fact, they're the inverse of each other. In some ways, you might say that the engineers who look at signals in the time domain and those who look at them in the frequency domain are the inverse of each other, too.

I'm talking about EMI engineers and digital designers. EMI engineers think in terms of emissions and look at signals with a spectrum analyzer. Digital designers (and some power-supply designers) often look at signals in the time domain, with oscilloscopes.

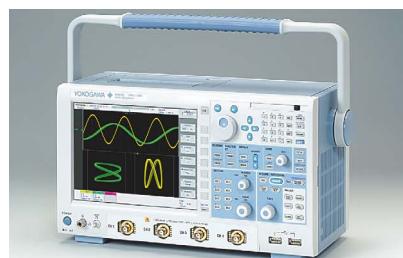
EMI consultant Daryl Gerke runs into situations where a circuit change that greatly affects the frequency domain shows little change in the time domain. In one case, a spectrum analyzer revealed excessive EMI in a product, but its designer and management were reluctant to alter the switching power supply's clock signal to improve emissions. "Show me on a scope that you haven't affected efficiency," the designer told Gerke. Gerke added a fer-

rite to the power supply's switching signal, which filtered the high-frequency harmonics that caused excessive emissions. (Most of the power is contained in the fundamental frequency and low harmonics.)

The designer in Gerke's story felt more comfortable working in the time domain than in the frequency domain. The same holds true for many digital designers, said signal-integrity consultant Dr. Howard Johnson. "EMI engineers should put their spectrum analyzer on a cart and wheel it to the digital design lab," he said. "Digital designers don't usually think about a circuit's frequency spectrum. They could learn from EMI specialists who use spectrum analyzers every day." Johnson also noted that digital designers often resist slowing their signal edges because

they fear increased jitter. With a better understanding of frequency-domain issues, designers can predict when to apply EMI filtering without affecting signal quality.

Doug Smith, a consultant in high-frequency measurements, often works on both EMI and signal-integrity issues. Smith said, "When you slow a rising edge in a digital data stream, look



Most engineers are comfortable with oscilloscopes, but fewer are comfortable with spectrum analyzers.

Courtesy of Yokogawa.

at an eye diagram to make sure that you haven't added excessive jitter." He also noted, "Many signals are faster than they need to be. A low-frequency clock with a fast rise time can cause more EMI problems than a signal with a higher fundamental frequency because of harmonics."

Smith said that all engineers should be comfortable with a scope and with a spectrum analyzer, but he added that you can learn a great deal about a circuit's integrity and EMI performance with just an oscilloscope. "Look at your signals. If you see repetitive noise riding on a signal, then check its frequency. It just might correspond to a power supply's switching frequency or to another signal."

Smith noted that too few designers take the time to see why a circuit works. Spend an hour or two with an oscilloscope, spectrum analyzer, or both to look at critical parameters such as jitter and noise. Measure common-mode currents, even when your design works properly. You'll have a better understanding of how your design works. **T&MW**

Troubleshooting guide CD



Keithley Instruments has compiled its collective measurement-troubleshooting knowledge into a free CD titled, "Interactive Test & Measurement Troubleshooting Guide: How to Avoid Common Measurement Errors." The CD covers low-level voltage, current, and resistance as well as high resistance and voltage from a high-resistance source. www.keithley.com/pr/018.

Low-cost signal generator

The SF800 from Signal Forge produces sine waves and square waves from 1 kHz to 1 GHz in 1-Hz increments. Waveform modulation capabilities include swept frequency with user-defined sweep rates, frequency modulation, amplitude modulation, frequency-shift keying, on/off keying, shaped on/off keying, asynchronous shift keying, and arbitrary modulation. Price \$985. www.signalforge.com.

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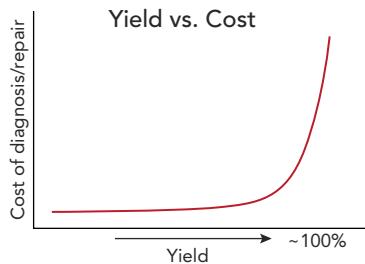


How much test is enough?

One fundamental question always haunts us: When are we finished testing? The answer is simple, at least in theory. We test products until they work.

Unfortunately, reaching that goal proves far more

complicated in practice. Last May, a major maker of embedded defibrillators announced that a flaw in some units could cause a small number of them to short-circuit and fail. In the days that followed, other makers admitted similar problems. All of them also announced that they had already



Especially in complex or high-reliability products, the cost of test and repair approaches infinity as the desired yield approaches 100%.

changed their manufacturing processes to eliminate the defects.

How could such failures happen? We invest enormous resources in test operations. According to one industry spokesperson who prefers to remain anonymous, the answer to "How much test?" depends heavily on the end application. Makers of medical goods, because of the grave consequence of field failure, resort to test steps that might include in-circuit test, optical and x-ray inspection, and functional test to make the overall strategy as comprehensive as possible. Computers and other less life-critical products would not require quite such fanatical attention.

Stig Oresjo, senior test-strategy consultant for Agilent Technologies, agrees with the consequence issue and proposes four other "c's": complexity, confidence, coverage, and cash-flow. The

first three define how much test you need. The last two—coverage and cash flow—serve as tradeoff indicators. Higher complexity (more defect opportunities) demands more comprehensive test.

Also, carefully consider your confidence that your test strategy accomplishes all of your goals. Estimating test coverage at any step includes assessing the cost of subsequent failures even before products ship to customers. Oresjo concludes that the dearth of easy answers is the main justification for test engineering.

John VanNewkirk, president and CEO of CheckSum, looks at "fitted" rather than "enough" test. He suggests fitting a test strategy to the product's fault spectrum in addition to its other

characteristics and advocates modifying the strategy based on that spectrum. Fitted test implies testing not only enough, but also for the right defects. Knowing the fault spectrum permits the use of layering test and inspection techniques so each can identify the faults that it can find most efficiently. VanNewkirk contends that some manufacturers concentrate too much on complicated "chimera" faults (that rarely occur), ignoring more common faults such as cold solder joints that their tools cannot find.

Yet—as with the defibrillators—no matter how carefully we plan, some faults get through. Preventing that from happening requires constant vigilance and a willingness to change strategies to incorporate new information. **T&MW**

REFERENCE:

"Maker of Heart Device Kept Flaw from Doctors," *New York Times*, May 24, 2005. www.nytimes.com.

IEST joins ISO nanotechnology committee

The Institute for Environmental Sciences and Technology (IEST) has been accepted as a voting member of the ANSI-accredited Technical Committee 229, formed by the ISO to address nanotechnology standards. Test methods will focus on physical, chemical, and structural properties of materials or devices whose performance is dependent on one or more dimensions less than 100 nm. wwwiest.org.

Book covers vibration and shock testing

Wayne Tustin of the Equipment Reliability Institute has published a new text covering environmental test topics. The 444-page book, *Random Vibration & Shock Testing*, discusses HALT, HASS, and ESS measurements, and it includes a CD-ROM with video clips and animations. Price: \$250. www.vibrationandshock.com.



Asset and ITT support Intel's embedded tests

Asset InterTech and International Test Technologies (ITT) report that they have jointly developed support for Intel Interconnect Built-In Self-Test (IBIST) embedded test technology on ITT's μ Master functional test platform. By combining at-speed processor-based functional tests and Intel IBIST-specific tests, electronics manufacturers can increase efficiencies and reduce test costs on boards based on Intel microprocessors. www.asset-intertech.com; www.intertesttech.com.

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BOOK REVIEW

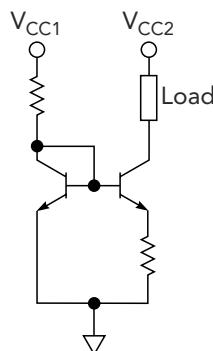
When you need current and voltage

Current Sources & Voltage References, Linden T. Harrison, Newnes (www.newnespress.com), 2005. 608 pages. \$59.95.

Need a stable reference voltage? Just get a zener diode and a resistor. Need a stable current source? Add a transistor and another resistor. That may be all you need, but circuit design isn't always that simple. For everything else, you'll benefit from reading Linden T. Harrison's book.

I've never seen a book devoted to these work-horse and often-overlooked circuits. *Current Sources & Voltage References* teaches you how semiconductor devices work

In *Current Sources & Voltage References*, Linden Harrison explains how to design these essential circuits.



and how to use them to design stable voltage and current sources. The author also gives you some history about the people that designed the early devices and circuits.

Harrison divides this book into the two topics, starting with current sources. For each of the two topics, he starts with semiconductor physics, moves on to device characteristics, and then on to circuit applications that build in complexity. He provides plenty of circuit examples, and he clearly explains how to use bipolar transistors, JFETs, MOSFETs, IC voltage references, and matched de-

vices in your designs. Harrison also spends several chapters covering classic devices such as National Semiconductor's LM134 current source and new devices such as the Advanced Linear Devices' ultra-low threshold CMOS transistor array, the ALD1107.

The book's application circuits go beyond the book's title. For example, Harrison explains how to use a voltage reference as a temperature sensor—the device's voltage is proportional to temperature. He also provides circuits that combine current sources with digital-to-analog converters to form a digitally controlled frequency source. (Disclosure: The book's publisher is owned by *Test & Measurement World*'s parent company.)

Martin Rowe, Senior Technical Editor

WEBCAST

Overcoming noise in data-acquisition systems

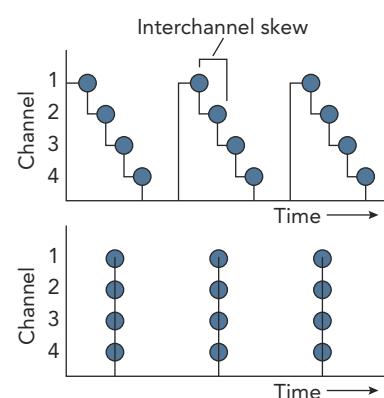
Data-acquisition systems, whether operating near DC or upwards of 1 GHz, can suffer adverse effects from seven types of noise:

- quantization noise,
- internal analog-to-digital converter (ADC) noise,
- power-line noise,
- time skew,
- aliasing noise,
- common-mode noise, and
- radiated noise.

In the Webcast "Overcoming Noise in Data Acquisition" (Ref. 1), Yusuf H. Chitalwala, Yokogawa product application manager, describes why these noise sources operate and explains how you can minimize their effects in applications ranging from low-speed machine monitoring to high-speed single-shot monitoring of destructive tests.

To reduce quantization noise, for example, Chitalwala recommends employing increased data-converter resolution as well as AC coupling in the presence of offset voltages. You can minimize internal ADC noise, he says, by employing a high-quality ADC, reducing the bandwidth you use, and maintaining a stable temperature.

To compensate for power-line noise, Chitalwala recommends using an integrating ADC, a moving-average software filter, a power-line filter, or isolated inputs. To handle time skew, he recommends simultaneous, rather than sequential, sampling, despite the latter's lower cost per channel. He describes aliasing in detail and recommends hardware filters as the best approach to eliminating adverse effects.



Sequential sampling (top) results in inter-channel timing skew, which simultaneous sampling prevents. An archived Webcast provides details.

He describes common-mode noise, which can plague thermocouple measurements of powered devices, and he

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Overcoming noise in data-acquisition systems (continued)

recommends the use of an isolation barrier to eliminate it. Finally, Chitalwala recommends shielding techniques for dealing with radiated noise.

Chitalwala wraps up by presenting an example of fuel-cell impedance testing. The example, which measures impedance increase (which degrades performance) over time, involves isolated inputs and outputs, 16-bit resolution, AC/DC coupling, programmable gain, and hardware filtering.

An archive of the Webcast is available on the *Test & Measurement World* Web site at www.tmworld.com/webcasts.

Rick Nelson, Chief Editor

REFERENCE

"Overcoming Noise in Data Acquisition: The 7 Deadly Sources and Improving the Measurement Performance of Any System," produced by *Test & Measurement World* and sponsored by Yokogawa's Test and Measurement Division, originally broadcast July 20, 2005. www.tmworld.com/webcasts.

MACHINE VISION

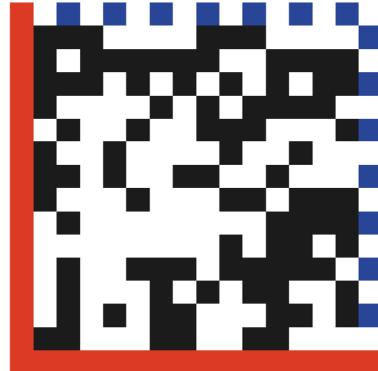
Testing direct part marks

Direct-part marking (DPM) is finding increasing use in the tracking of electronic components as they pass through a manufacturing process. The article "How do you make your mark?" (Ref. 1) covers some basics of how to choose the appropriate marking technology and symbol format (such as a 2-D Data Matrix code), how to decide what information to store in your chosen symbol, and how to make sure your symbol technology is compatible with your production processes.

But if you've determined that permanent DPM (as opposed to the use of a removable label) is right for you, you'll need a way to ensure that the mark you affix is of sufficient quality to remain readable throughout the manufacturing process and beyond. According to a 16-page report from Cognex (Ref. 2), "Because the quality of a direct marked 2-D code is so critical to the success of lifetime part traceability, many manufacturers view the 2-D mark as a critical attribute of the part itself."

Ensuring code quality requires verification of the various matrix segments, including the finder pattern, clock track, and data region (figure), as well as the "quiet area," or the clear area that surrounds the pattern on all four sides.

The Cognex report provides details on what you need to know about symbol quality, presenting topics ranging from a standards overview (including information on the ISO 15415 print-



A Data Matrix symbol includes a finder (L) pattern (red), a clock track (blue), and data modules or cells (black), whose quality must be verified. The colors are for illustration purposes only; the actual symbol would be monochromatic. *Adapted from Ref. 2.*

quality specification and its limitations for DPM applications), to implementation issues (including camera resolution, lighting, and fixturing). It also describes available DPM verification systems, including in-line, stand-alone, and handheld models.

Rick Nelson, Chief Editor

REFERENCES

1. Titus, Jon, "How do you make your mark?" *Tech Trends, Test & Measurement World*, July 2005. p. 19. www.tmworld.com/archives.
2. "Implementing Direct Part Mark Verification: 10 Important Considerations," Cognex, 2005. www.cognex.com/dpm.



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*Source: iSuppli, Nov. 2004



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THE TOOLS

- CKC Labs: EMI testing lab. www.ckclabs.com.
- Com-Power: spectrum analyzer. www.com-power.com
- ETS-Lindgren: EMI receiving antenna, EMI test chamber. www.ets-lindgren.com.
- National Technical Systems: EMI testing lab. www.ntscorp.com

PROJECT DESCRIPTION

DPS Telecom (Fresno, CA) designs and manufactures telemetry equipment used to monitor telecommunication networks and remote site environments. When customers started asking DPS to provide NEBS-compliant products, the company encountered unacceptable delays from using outside testing labs to perform pre-compliance electromagnetic interference (EMI) testing.

DPS engineers didn't just buy an EMI test chamber, equip it, and say, "problem solved." They first built an experimental chamber with wood and chicken wire and used a radio to determine if the cage reduced outside signals. They could then perform relative radiated and conducted emissions measurements. "When we first started performing our own EMI tests," said project manager Ron Stover, "we literally locked an engineer in the chamber because it didn't have any doors."

With the experimental chamber, engineers learned how to reduce emissions. "At first," said Stover, "we had to meet standards by using filtering and grounding in our chassis." Eventually, by reading books and attending seminars, the staff learned to design for low emissions. With a successful proof of concept, the DPS engineers were ready to pursue their goal of eliminating the need for an outside test lab for precompliance tests. DPS then purchased its own 4x8-ft EMI chamber that the engineers later expanded to 4x16 ft so they could perform 3-m tests.

DPS engineers redesigned existing products at the board level to reduce emissions, which eliminated the need to add ferrites and other components to their chassis. "Today," noted Stover, "there's very little difference in emissions, whether we have the chassis cover on or off. Once in a while, we put an old product into the chamber to verify that the test equipment works because new boards are so quiet."

After setting up the purchased chamber, the DPS engineers brought their measurement equipment—an EMI antenna and a spectrum

analyzer—to a test lab and tested a product. Then, they went back to their chamber and retested the product. Doing so let them prove that tests done in their chamber would be consistent with those performed at an outside lab.

During a precompliance EMI scan, DPS engineers simulate the signals that a product sees in actual use. They exercise the Ethernet and RS-232 ports by connecting them to a computer and running diagnostic software. A manual switch box lets them simulate signals from external alarms.

DPS engineers develop eight to 20 new products each year, and they get those products



An EMI chamber lets DPS engineers perform precompliance tests in house. Courtesy of DPS Telecom.

to market four to eight weeks earlier with the in-house chamber. They use an outside lab for compliance certification with a high level of confidence.

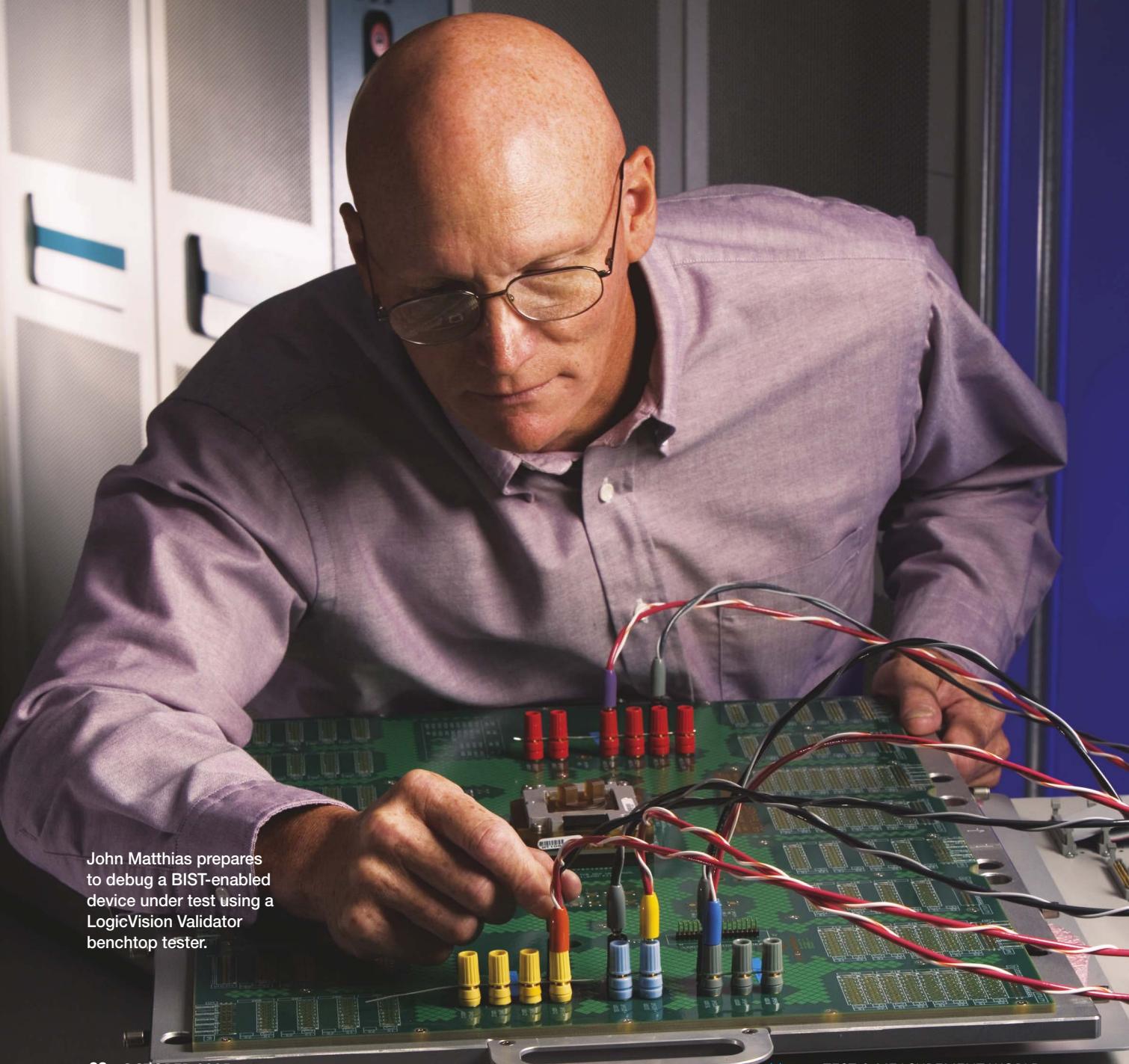
LESSONS LEARNED

Through building a preliminary chamber and studying the fundamentals of designing for compliance, DPS engineers learned that designing for NEBS compliance at the start makes their products less expensive to build and gets them to market faster than trying to retrofit NEBS compliance into existing designs. They've learned how to design quiet boards while using a minimum of ferrites and other components—which can add to a product's cost—to suppress emissions.

Martin Rowe, Senior Technical Editor

DESIGN

EFFECTIVE COMBINATIONS OF ATE, BIST, AND DFT



John Matthias prepares to debug a BIST-enabled device under test using a LogicVision Validator benchtop tester.

MEETS TEST

HELP AGERE SYSTEMS GET QUALITY CHIPS TO MARKET FAST.

RICK NELSON, CHIEF EDITOR

ALLENTOWN, PA—Developing an effective design and test strategy for an IC can be a daunting task. At Agere Systems, the difficulties are magnified because the company produces hundreds of distinct devices, with 200 or so designs having been completed within the past year and a half. Each product benefits from a particular design and test strategy, which involves identifying an appropriate ATE system as well as an optimal combination of design-for-test (DFT) and built-in self-test (BIST) technologies.

Supporting the company's four divisions—Enterprise & Networking, Mobility, Storage, and Telecommunications—Lou Ternullo and John Matthias are part of teams that serve as central resources that can help each division most effectively meet its design and test goals. Ternullo, technical manager for DFT and IP in the company's design-platform organization, is responsible for BIST and DFT tools, while Matthias, distinguished member of the technical staff in the IC test technology group, is responsible for automated test equipment (ATE) and benchtop debug tools.

Ternullo explained, "My team's charter is to stay on top of the DFT tools that are available in the market. At the same time, I work with John's team," which is concerned with the back end of the production and test process, "to ensure that design and test tools play well together." Because no team has the resources to extensively evaluate every DFT and BIST tool on the market, he said, "We try to intelligently determine which DFT tools may add value to our flow through press articles, news releases, and of course, vendor visits."

What's up-and-coming now, he said, are more advanced automatic test-program generation (ATPG) tools, which include at-speed ATPG and compression techniques in addition to BIST tools, such as ones from LogicVision.

Agere employs a combination of electronic design automation (EDA) tools, and Ternullo cited the benefits of a multivendor approach. "We have contracts with multiple EDA vendors," he said, adding that multiple sets of tools help to provide a good balance to help Agere's design team meet various design challenges. "Vendor A's tools may work better to help meet a customer's specification on one design," he said, "whereas vendor B's tool may prove to be better for a different design. In addition, one vendor's tools may be more up to date with respect to certain features." Having multiple vendors, he added, also helps to increase competition, which in turn fosters regular tool improvements.

He also noted that in addition to having expertise in available commercial tools, Agere, with its AT&T Bell Labs and Lucent heritage, can apply its own technologies. "We had our own DFT development team years ago, with our own ATPG, logic BIST, memory BIST, and boundary-scan tools. Having the knowledge from our DFT tool development days helps my team better assess the value-added features in the tools we use and evaluate. We like to stay on par with our vendors in order to add value for our customers."

(continued)



A modified board employs banana jacks and other connectors to provide a Validator benchtop system with access to power and ground planes, high-speed clocks, and the test access port.

ED WHEELER



SEMICONDUCTOR TEST

Using memory as an example, he said, "We work with DFT vendors who typically do not have memory expertise as well as memory-design companies and compiler companies that typically do not have DFT expertise. In working closely with them, we ensure that their solutions, first, fit into our flow and, second, are being used optimally to test our chips. We work with them on adding value to their tool. We do a lot of testing of beta code on new releases of software, and there's a lot of give and take. They won't do everything we request. But the features they agree to develop help add value to Agere designs."

In cases where vendors cannot provide Agere with a cost-effective solution, Agere designers sometimes rely on internal expertise. For example, Ternullo said, "One customer required the use of a ternary CAM [content addressable memory] in its design, and no commercial tool vendors offered a competitive BIST solution. That's where our in-house expertise paid off. We internally developed a BIST engine to test ternary CAMs. Developing our own BIST controller is not always the most practical solution, but it's one way Agere can add value to its DFT offering."

Serving internal customers

Knowledge of available commercial tools and in-house expertise helps Ternullo's group meet its primary goal, which, he said, "is to support our own customers, which are the internal divisions here at Agere, throughout the DFT flow. Our efforts begin with what we call test architecture review." Within the design community, he said, there's persistent resistance to DFT and BIST unless "it has no impact on area and performance, and we know that's not possible. But we can minimize DFT disruptions by working with chip architects early on to map out functional blocks and determine how to interface them with the test technologies we plan to use. Early involvement will help avoid the need to repartition the design to accommodate DFT further downstream in the design cycle when it becomes more difficult. We continue working with chip designers throughout the DFT insertion process to help improve Agere's chances of success."

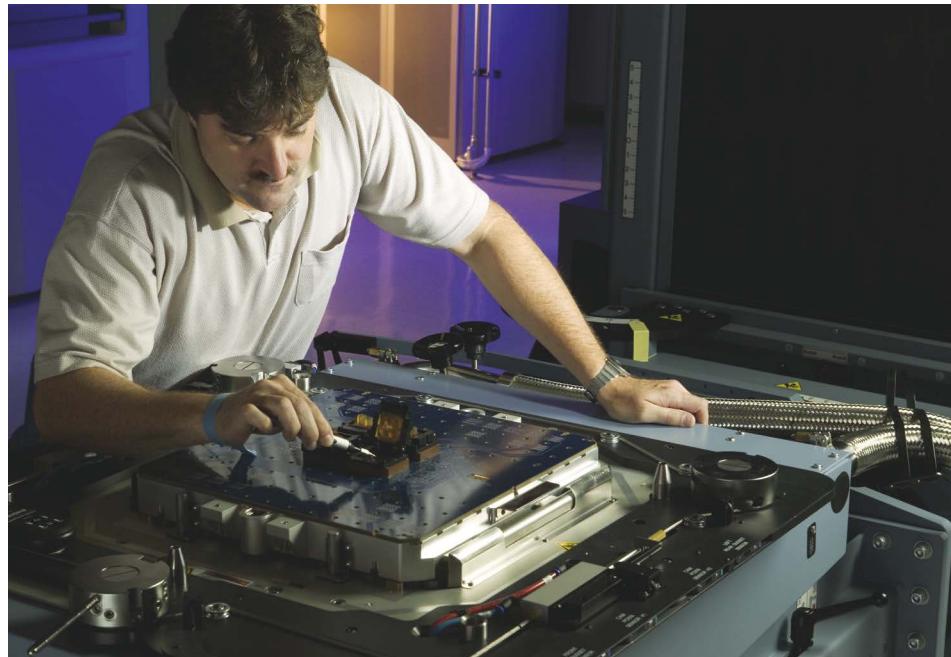
The exact status of a design when Ternullo's group gets involved depends on the product line. "Agere has what's re-

ferred to as 'standard products' and ASICs. Agere develops standard products internally and typically has access to all the RTL code. On an ASIC product, we typically start with a gate-level netlist. Whatever the case, we like to see at least a high-level block diagram that provides some general idea of the partitioning.

"When we do get to the floor-planning stage, we may modify the logical or physical partition. For example, we will

ing messages might suggest such a tool exists, but Ternullo and Matthias both agree that it doesn't. Said Ternullo, "Part of what my team does is cut through the marketing fluff and see where the rubber meets the road." One tool, he said, might make it very easy to insert DFT, and that tool would make designers happy by getting to tape-out quickly. "But if as a result of using that tool it takes weeks to bring the test program up on an ATE system,

ED WHEELER



Doug Rabold, test center facilities engineer, sets up a Teradyne UltraFlex, one of approximately 35 ATE systems used for test development at Agere's Allentown test facility.

attempt to share memory BIST controllers as much as possible between like memories to reduce area, or we may make tradeoffs in test time by testing some memories serially and others in parallel. These are all tradeoffs we address up front. We can't know for sure that we've made the right choices until we achieve timing closure, but by being involved from the beginning, we can minimize the number of iterations required to complete a DFT-inserted design."

Of course, multiple-vendor flows do have drawbacks. Said Ternullo, "We would love to have one tool set that would satisfy our DFT needs from end to end in the design process—allowing us to do analysis at the front-end architecture level all the way to the back end, including field returns." EDA vendors' market-

then the savings gained on the front-end are wasted." The same is true for the reverse, he added, where the savings of an easy-to-bring-up test program might be more than offset by a difficult, costly, and time-consuming DFT-insertion phase.

So, said Ternullo, his team evaluates the effect of a tool from architecture conception, DFT and BIST insertion, and validation to bringing up first silicon, debugging it, and developing production-test programs. To that end, he works closely with Matthias, who said, "We are tearing down the wall between design and test. Maybe it's not 30 feet high anymore, but it's still there." Said Ternullo, "John and I are in totally separate organizations, with our reporting chains meeting at the executive level. But we do not let that get in the way of



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doing what is right for Agere. We work together to resolve issues to the benefit of both the front-end and back-end teams. A lot of what we do is internal marketing to the divisions."

Supporting production

For his part, Matthias is part of the global operations team, which supports manufacturing, beginning at the point where a product tapes out and continuing throughout the production life cycle. Agere has adopted a "fab light" strategy, in which it increasingly employs external foundries, but it nevertheless retains about 95% of assembly and test functions in house. Agere does outsource some packaging and test of some high-volume parts, but

Matthias said that keeping test in house is cost-effective and makes it easier to serve end customers, who are putting packaged parts or bare die on printed-circuit boards. With the test function in house, he said, Agere can quickly respond if customers experience a problem such as high line fallout or high return rates. "We can get involved quickly to get to the root cause of the problem."

Matthias said global operations includes everything from supply-chain management to shipping. Within that operation, he said, "My particular group, test technology, is a very small group of experienced people who have been in the test world for typically 15 years or more.



Agere Systems' 31,000-ft² test facility in Allentown employs more than 100 test professionals, including telecom test engineer Charles James, who is shown here working with an Agilent 93000 system.

One of our primary responsibilities is forward-looking—what's the next technology we have to prepare for? What's the next type of product we will manufacture, and what equipment will we need to test it?" To prepare for future products, he studies the internal roadmapping of Agere's design teams and keeps tabs on what ATE and EDA vendors are doing. "We are very proactive with our ATE vendors, working with them 12 to 18 months ahead so that we can get them on the same roadmap for developing their tools to support what we have coming."

Matthias continued, "Anything we believe will give us an advantage in getting product to market faster and resolving

customer problems faster is something that I am interested in. So, I work really closely with Lou, and I get involved early with some of the design teams." He tries to head off problems such as an engineer embarking on a design that might require a 10-Gbps signal from an ATE system. "I say, time out. Let's discuss your specific test needs, what the ATE can provide directly, and what we might need to augment with other components or instrumentation. And we work out test strategies that we can support with our existing production equipment."

Is there a move within Agere to outsource assembly and test, as some companies do (Ref. 1)? According to Matthias, "We've been

doing [assembly and test] internally for a long time and have a large installed base of capital equipment. We've evaluated this extensively, and our conclusion has always been the same: there are key advantages to maintaining these functions in house. We do outsource some amount of assembly and test, but we still see significant economical and operational advantages to keeping a major portion of this function in house. The test houses have flexibility in that they have a lot of different equipment and are willing to reconfigure it to test a certain product, but they don't necessarily have the test-development expertise we have, and they certainly don't have the knowledge of

Failure analysis

Consulting member of the technical staff Bob Pajak summarized operations in Agere's failure-analysis lab, which include a variety of nondestructive techniques as well as package and die deprocessing, device test, and early design debug and analysis. Available equipment includes scanning electron microscopes for observing physical defects. In addition, various probe systems are available to acquire internal device waveforms. So, too, are focused-ion-beam systems, which can establish probe points to bring signals to the DUT surface and which can perform circuit-editing functions, as well as ATE systems, which provide stimulus to a DUT. In addi-

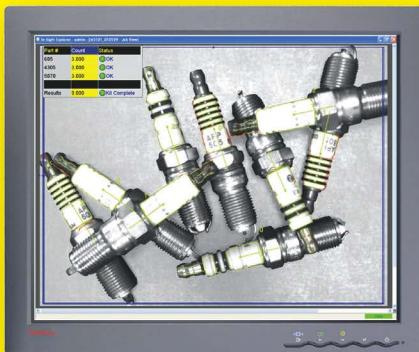
tion, he said, engineers use desktop debugging systems including the LogicVision Validator and the Teseda V520 to help isolate problems.

Dale Yoder, an engineer with the storage product group, described how he uses the Teseda system. "I'll get a red light from ATE on the test floor, and I can bring the part back to the lab where I can quickly run sets of vectors, truncate them, run loops, and perform DC and even some AC scan." He said he can work with Teseda's OpenDFT Workbench software as well as Synopsys TetraMAX to isolate a fault to a specific node, often in a matter of seconds.—Rick Nelson

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the device design. By keeping these functions in house, if a problem arises, we don't have to try to coordinate our troubleshooting efforts across multiple different companies."

Matthias cited as an example a defective-parts-per-million (DPPM) problem in a customer's production line that re-

sulted in elevated levels of field returns. "We've done a lot of ASICs for modems and Ethernet cards that are being sold to consumers by the millions. If you buy a modem or network-interface card from company A and it doesn't work, you send it back to company A. If company A's engineers identify what they think is a

DPPM problem with a part that we supplied, then we get involved. I have actually gone to customer production facilities to investigate their production lines and help resolve such issues—not to say, 'it's your problem, not mine,' but to get to the bottom of whatever the problem is. We've found the gamut of issues: Some have been assembly-related, some have been test escapes, some have resulted from design issues, and some have been customer production-line issues. Whatever the cause, we pull in a lot of experts to help our customers solve their problems as quickly as possible."

What does Agere's ATE lineup look like? According to Matthias, "We've done a lot of work in controlling costs internally over the last few years and have migrated from about seven different ATE vendors down to primarily two—Agilent and Teradyne—although we still have some legacy equipment." Why not stan-

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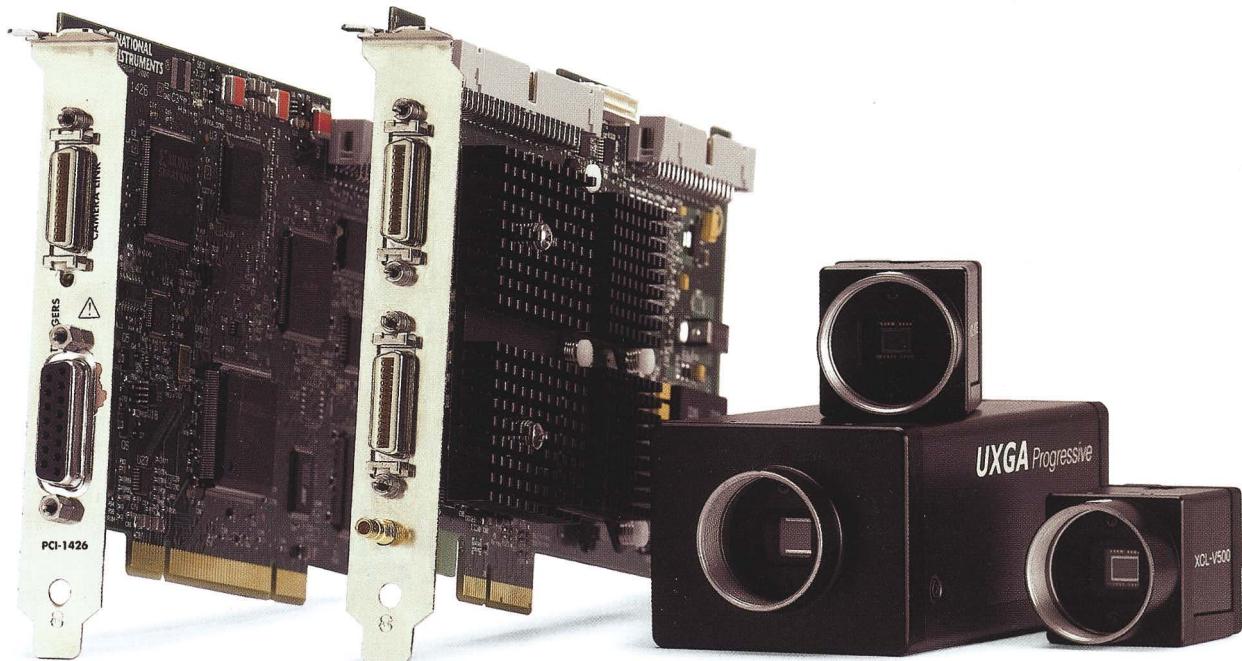
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dardize on just one? "We continue to look at that issue, but we believe there is a healthy environment created by competition. So, not only from price perspective but also from a technology perspective, we see a lot of benefit in driving a couple of vendors toward the same goals." Some test development is done at remote locations, but most is done in the 31,000-ft² Allentown test facility, where 35 ATE systems mirror the testers that Agere has deployed around the world. More than 100 test engineers working for the various business units develop test programs.

Matthias added that there can be a downside to standardizing: "When you try to narrow down to a very small number of providers, a lot of times you'll miss players in niche markets—for instance, one that makes a very small, compact RF tester that does the job very well. It's a give and take—you have to constantly keep looking at things. From a pure product-line perspective, it makes sense to go out and pick the best equipment set for your particular product, and we were on that path in the past, but from a manufacturing perspective and a support perspective, that's the most difficult thing to do—you have to support all the interfac-

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Sony Introduces LINE OF Camera Link CAMERAS

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The ultra compact XCL-V500 and the XCL-X700 black-and-white cameras feature a $\frac{1}{3}$ -type progressive scan CCD that captures high-quality monochrome images in square pixels. Both models feature partial scan and a binning function to further increase the frame rate. The XCL-V500 and XCL-X700 cameras measure only $1\frac{3}{16}$ in. by $1\frac{3}{16}$ in. and weigh only two ounces for easy installation in space-restricted environments.



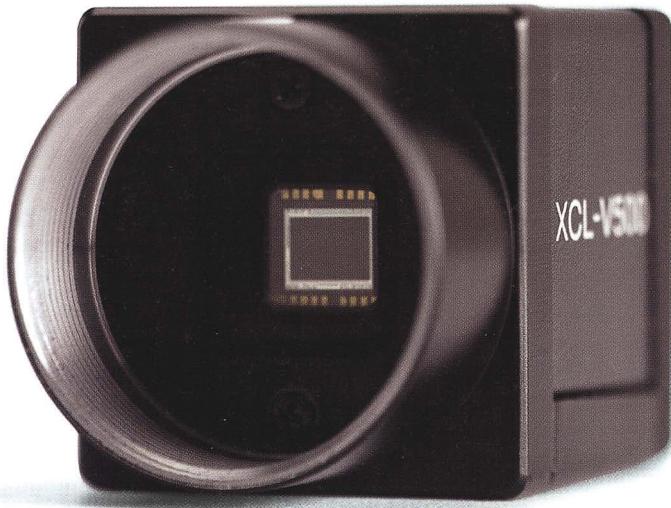
XCL-V500 CAMERA

The XCL-V500 offers a VGA image (648 by 494 pixels) captured at 60 frames/s. The external trigger shutter speed is $\frac{1}{4}$ to $\frac{1}{10,000}$ seconds.



XCL-X700 CAMERA

The XCL-X700 offers an XGA image (1,024 by 768 pixels) captured at 29.2 frames/s. The external trigger shutter speed is $\frac{1}{4}$ to $\frac{1}{10,000}$ seconds.



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XCL-U1000 Camera



The top-of-the-line model, the XCL-U1000 black-and-white camera, measures only $1\frac{3}{16}$ in. by $2\frac{1}{16}$ in. by $3\frac{3}{16}$ in. and incorporates a $1/1.8$ -type progressive-scan CCD that produces detailed, ultra extended graphics array (UXGA) resolution images (1,600 by 1,200 pixels) at 15 frames/s.

XCL-U1000C Camera

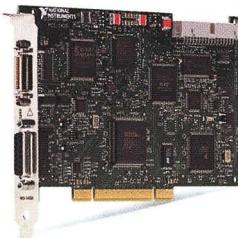


The XCL-U1000C adds a color "mask" (commonly known as a Bayer filter) and a digital signal processor to the CCD to provide uncompressed, high-resolution color images. The XCL-U1000C also has a binning function, white balance, and a matrix function.

To access data sheets, videos, and other technical resources visit, ni.com/info and enter code **camlink**.

What is Camera Link?

Camera Link is an industrial, high-speed, serial data and cabling standard developed by National Instruments, camera vendors, and other image acquisition companies. Created for easy connectivity between the PC and the camera, Camera Link provides simple, flexible cabling for high-speed, high-resolution digital cameras. A Camera Link cable is a slender, 26-pin cable with 24-bit data, clock, and enable as well as control signals. You can control camera functionality by asynchronous serial control or LVDS differential lines through a Camera Link cable. Camera Link comes in three configurations – base, medium, and full. The base configuration uses three 8-bit taps, or input channels, to acquire up to 24 bits of data at a rate of 255 MB/s. The full configuration offers eight taps and can acquire images up to 680 MB/s.



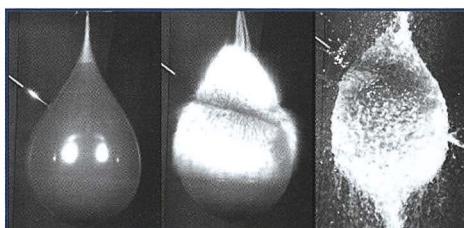
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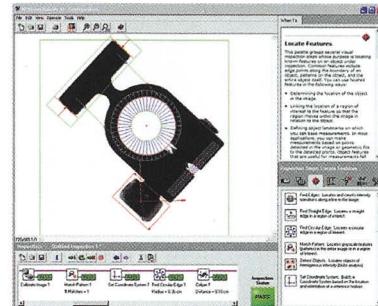
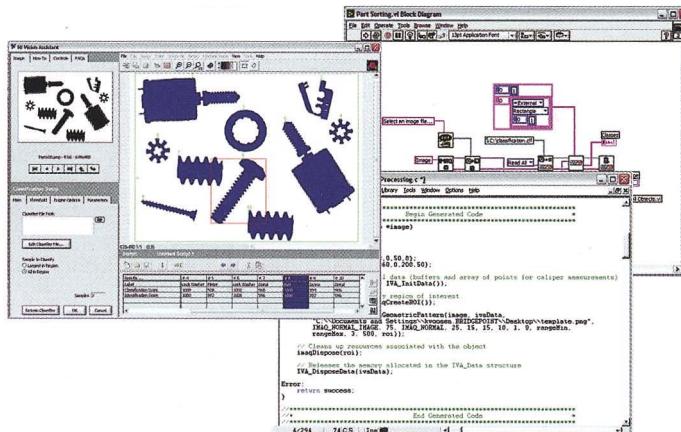
NI Vision Software

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ing, all the docking, and all the software for all these different platforms, and it just becomes unmanageable very quickly."

Testing high-mix products

A particular challenge, Matthias said, is how to cost-effectively test high-mix products. "Many ATE solutions involve changing pin cards in a test head. That approach might work well for a business that has relatively few line items running at high volumes. But it doesn't work well for other businesses that tend to have many more line items with different testing needs and lower-volume line items. This week, I might need to test 30,000 parts from one product line, but then I might have to take that tester off-line to switch out pin cards to reconfigure it for a different product that I need to test next week. The end result is a lot of down time and a big hit on machine utilization. To combat this, we try to deploy our equipment with a rather broad configuration that we can use for many different product types." Sometimes, he said, this approach might complicate things like load-board design, but it gives Agere a lot better equipment utilization in its factory.

He added, "DFT plays a big role in our strategy as we move away from the days of pure functional test, where it could take a year to develop a test program." DFT and BIST, he said, enable rapid test-program development and test-program conversions, allowing the company to quickly put a product on a different platform to manage production spikes. "We are really trying to capitalize on the DFT investment that we've made at the front end and take maximum advantage on the back end. We are making a lot of progress there. It's a good news story for us."

Despite a streamlined tester lineup, ATE is still an expensive resource, and Matthias tries to avoid tying up a system intended for production-test-program development to perform silicon debug or failure analysis. To that end, he has enlisted benchtop systems from companies such as LogicVision and Teseda for debug and other tasks (see "Failure analysis," p. 32). In particular, he noted that Agere has used the LogicVision Validator to quickly bring up first silicon containing LogicVision BIST.

Of course, desktop debug units require a physical interface to a device under test

(DUT), and using such a unit can require a special debug load board in addition to a production load board. With such boards costing \$5000 to \$10,000 and requiring a 5- to 8-week cycle time, that's a discouraging prospect. To eliminate the need for a debug load board, Matthias employs production ATE boards designed to facil-

itate use with the LogicVision Validator. The modified board employs various connectors to provide access to power and ground planes, high-speed clocks, and the test access port (TAP). It's been a tough sell to production-test personnel, he said, who don't care to see any modifications that could conceivably interfere with pro-



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duction tests. To assuage their fears, he employs high-speed relays to provide a clean path to the ATE and to switch out connector access routes so the related load-board traces don't serve as stubs that could compromise measurement results.

With the Validator, Matthias can perform debug as well as help with test-

program development. For example, he said he can experiment in real time with reordering tests to decide which ones to run in parallel (which minimizes test time at the expense of potential power problems) and which to perform serially (which minimizes power but extends test time).

The modified-load-board scheme works well with the minimal interface requirements of the Validator, but it's not appropriate, Matthias said, for use with the Teseda V520, which requires a high-density, 300-pin interface that Matthias doesn't believe is appropriate to add to a production load board. For the Teseda box, a custom interface board is his preferred solution, although he continues to experiment with designs for a generic solution that would take advantage of the existing DUT card designs used for physical failure analysis at Agere.

ATPG or BIST?

While the LogicVision Validator box is designed to support BIST solutions, the Teseda box is designed to support ATPG solutions, both of which are in widespread use at Agere, Matthias said, adding that "from a test perspective, BIST is very attractive due to the small number of pins, minimal ATE requirements, and built-in diagnostics. BIST is well-suited to lower-cost DFT-based testers."

Nevertheless, some controversy swirls around the BIST vs. ATPG decision. See, for example, the comments in favor of ATPG by Robert Hum, VP and GM of Mentor Graphics design verification and test division (Ref. 2), and the response of LogicVision president & CEO Jim Healy (Ref. 3).

But neither Ternullo nor Matthias is dogmatic with regard to the issue, and both expect ATPG and BIST approaches to find use. According to Ternullo, the optimum test solution for any product will depend on the fault coverage it provides as well as on how well it is integrated with front-end EDA tools and back-end debuggers and ATE systems. Ultimately, the choice will center on what best serves Agere's customers. Concluded Matthias, "At the end of the day, our number one goal is keeping the customer happy. Customer satisfaction is paramount." **T&MW**



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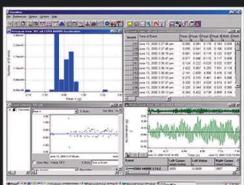
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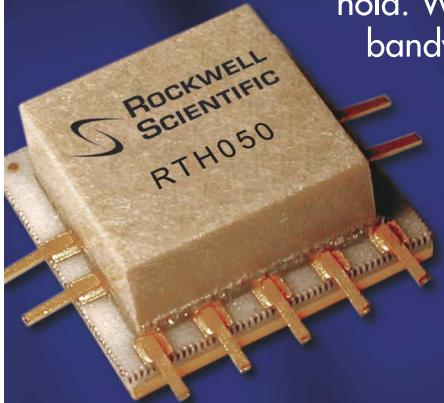
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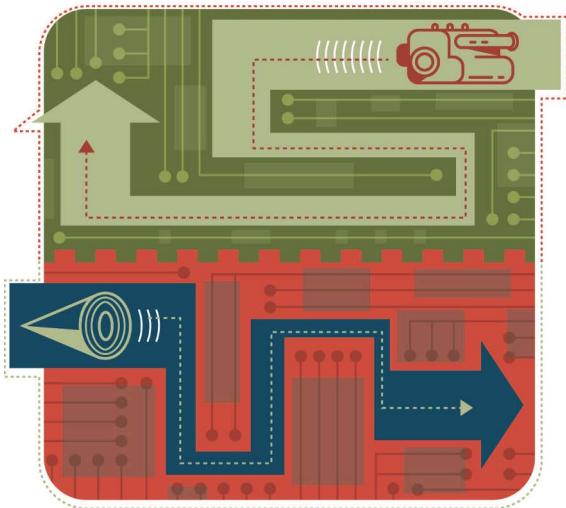


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IEEE 1149 EXPANDS DIFFERENTIALLY



THE VENERABLE STANDARD ADDS SUPPORT FOR THE DIFFERENTIAL SIGNALS FOUND IN SERIAL BUSES.

BRIAN STEARNS, NATIONAL SEMICONDUCTOR

Serial buses, which provide the bandwidth needed to bring streaming audio and video to computers and communications systems, are replacing the parallel buses that typically traverse cables and backplanes. To achieve the bandwidth necessary to keep the data bits flowing quickly, serial buses use AC-coupled, differential signals, a technique that complicates the testing challenge.

The IEEE 1149.1 boundary-scan (JTAG) standard was sufficient for testing parallel, single-ended networks, but it is useless for testing AC-coupled differential networks. The IEEE has addressed this limitation with IEEE 1149.6, which extends the boundary-scan standard to handle the signaling in today's serial buses (Ref. 1).

Serial vs. parallel

Parallel, TTL-level buses have widened to 64 bits, but their low bandwidth (tens of megahertz) limits their usefulness. Physical space and switching noise prevent parallel buses from keeping up with bandwidth demand.

PCI Express, Fibre Channel, Serial ATA, and other serial buses consume far less physical space than their parallel cousins. They use serializer/deserializer (SerDes) devices to serialize multiple channels of parallel TTL-level signals into a single high-speed data stream. At the receiver, another SerDes device deserializes the serial stream back to TTL-level (single-ended signaling) channels (Figure 1).

For an 8-bit TTL bus that operates at 66 MHz, a SerDes device can convert the bus to a serial stream operating at a 528-MHz data rate. In reality, the bus will need as much as 1 GHz of bandwidth to cover the overhead associated with sending the data in packets. In a serial configuration, the number of conductors drops from eight to two, which reduces signal noise and saves board space. Many IC manufacturers provide a variety of SerDes functions using an assortment of technologies, including low-voltage differential signaling (LVDS), current-mode logic (CML), and low-voltage positive emitter-coupled logic (LVPECL).

To eliminate threshold offsets, engineers AC-couple serial signals by inserting capacitors into the high-speed interconnects between drivers and receivers. AC-coupling also eliminates ground offsets if the driver and receiver are on different cards or use different power supplies. The capacitors act as a high-pass filter, eliminating the DC bias of the signal while passing the high-speed signals. To further maintain DC balance in the data stream, most high-speed SerDes devices use an 8b/10b encoding scheme, which keeps the number of 1's and 0's roughly equal.

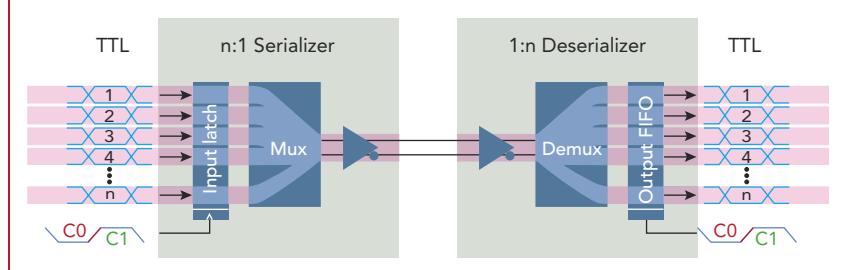
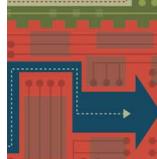


FIGURE 1. Serializers and deserializers help migrate single-ended TTL to high-speed differential signals.



Test issues

With single-ended TTL buses, you can use IEEE 1149.1 to verify the connections. As long as a system contains JTAG-enabled drivers and receivers, you can sufficiently check the integrity of these single-ended connections using basic JTAG techniques.

The IEEE 1149.1 standard, however, was never intended for differential networks. It falls short in environments that contain frequency-dependent parasitic components. At the higher data rates of the differential environment, the conductors behave like a transmission line, and you must include all the frequency-dependent parasitic components in any model of the serial bus. This makes de-

tively simple products because it adds cost and complexity. It is also a synchronous approach, but simple buffer and switch components don't otherwise require a clock. A standardized pseudo-random pattern is still required to use at-speed BIST across products from different vendors. At-speed BIST produces pass/fail test results without any diagnostic capability.

Enter IEEE 1149.6

To address the issues associated with testing AC-coupled interconnects, the IEEE developed IEEE 1149.6. This standardized test approach makes interoperability of 1149.6 features across vendors and across differential interface technologies

the differential pair can operate within the normal common-mode range of the receiver.

Design challenges

To maximize IEEE 1149.6's effectiveness, the circuitry in a compliant device must not impact the device's mission mode (normal operation), especially the basic parameters of the individual signaling standards. Some minor impact to the receiver input structure such as a slight increase in output delay or added leakage or jitter might occur. The additional circuitry needed to support 1149.6 is manageable—providing the circuit designer is aware of the potential impact (Ref. 2, 3).

A second challenge comes in designing a methodology that will detect all possible faults in the high-speed interconnect. Although IEEE 1149.6 is intended as a universal solution for differential signaling, the implementation that works best in one termination scheme may not be the best approach for all termination schemes and all faults. There are a wide variety of differential interface technologies, and each requires a unique implementation because each has a unique fault dictionary. The various implementations of termination schemes and receiver fail-safe circuitry also add to the complexity of the fault dictionary. The best approach to address this challenge requires collaboration between the ATPG software vendor, the chip designer, and the board designer. **T&MW**

FIGURE 2. Capacitors pass pulses from a transmitter to a receiver

tection of frequency-dependent faults more difficult when using single-ended IEEE 1149.1 test approaches. In addition, AC-coupling blocks DC 1149.1 test patterns, rendering it completely ineffective.

A unique feature of some newer multichannel high-speed SerDes products is an at-speed built-in self-test (BIST) mode that can test the high-speed signal path. This test mode is sufficient for evaluating interconnects at the system operating speed (not at the slower test speeds), and it also works in an AC-coupled environment. At-speed BIST can be initiated and verified using the IEEE 1149.1 architecture.

For at-speed BIST to work, a serial bus must have a driver and receiver from the same vendor, a setup that is not always practical to implement. Although simple buffers and switches have become more popular for improving signal integrity of FPGA I/O or for boosting signals, at-speed BIST isn't efficient in these rela-

possible. Its simple implementation makes it practical for testing even basic PHY devices. Furthermore, software tools can provide comprehensive diagnostic capability for the targeted fault dictionary.

An IEEE 1149.6-compliant driver must incorporate the circuitry to generate high-speed pulses, initiated on IEEE 1149.1-delivered instructions (Figure

2). These high-speed pulses will pass through the coupling capacitors, and an 1149.6-compliant receiver

must detect the pulse edges and provide a pass/fail indication through the IEEE 1149.1 interface.

IEEE 1149.6 adds two opcodes, EXTEST_PULSE and EXTEST_TRAIN, that you can use to activate test modes. EXTEST_PULSE initiates a single pulse. EXTEST_TRAIN sends a series of pulses from the driver to the receiver, and it lets you charge the transmission line when you don't use an external reference. You must charge the line so

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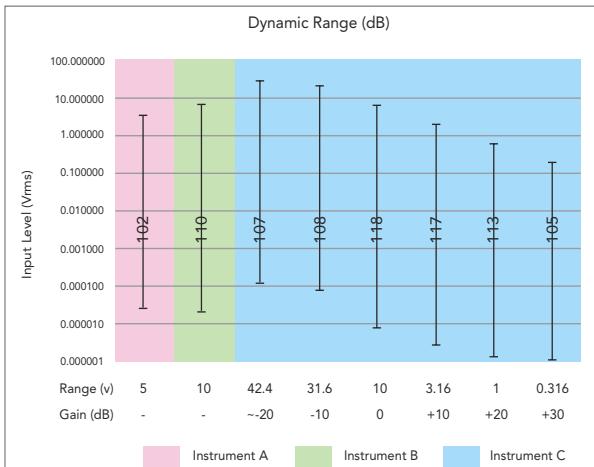


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Almost everyone has heard the difference in the quality of sound produced by movie-theater system and that produced by home-theatre audio equipment. The difference can arise from audio-signal distortion that human ears can detect at low levels. Thus, rigorous testing must occur during product design and during manufacturing to ensure companies ship good MP-3 players, cell phones, sound cards, and so on. Testing involves measuring many characteristics, such as signal-to-noise ratio, total harmonic distortion, dynamic range, and intermodulation distortion.

Although distortion may seem like a qualitative criterion, instruments can readily measure energy at harmonic frequencies that we hear as distorted sound. To help quantify distortion, engineers use instruments that detect low-amplitude signals produced by combinations of standard test signals in audio electronics. Intermodulation distortion (IMD) measurements, for example, compute the ratio of the root-mean-square (rms) value of two test signals, f_1 and f_2 , to the rms value of "products" that arise from mixing or modulating the two test signals. Signal



The plot above shows the range of measurement voltages and the corresponding dynamic range for three instruments. Instrument C offers six gain settings. Note the dynamic range varies from one gain setting to the next.

mixing takes place in non-linear circuits and components that exist to some extent in all electronics. Second-order IMD frequencies exist at f_2+f_1 , f_2-f_1 , $2f_2$, $2f_1$. Third-order IMD frequencies exist at $2f_1+f_2$, $2f_2-f_1$, f_1+2f_2 , and f_1-2f_2 . Good design and testing techniques ensure electronic equipment produces harmonics at low levels, which minimizes distortion.

Often, the second-order IMD frequencies exist some distance from f_1 and f_2 , but two third-order IMD frequencies occur close

to f_1 and f_2 . Thus, filtering can remove second-order IMD components but not third-order IMD frequencies, which exist too close to f_1 and f_2 . The change in amplitude of the test signals f_1 and f_2 also affects the amplitude of the IMD-generated signals. An increase of 5 dB in a fundamental frequency increases the amplitude of its second harmonic by 10 dB and the amplitude of its third harmonic by 15 dB. To ensure IMD frequencies will not distort audio signals, engineers require audio test equipment that can accurately measure IMD frequencies over as large a dynamic range as possible.

Dynamic range expresses how well an instrument can detect small signals in the presence of large signals. Because an IMD measurement requires simultaneous measurement of stimulus signals and their low-amplitude harmonics, instruments require a wide dynamic range. The comparison of the largest mea-

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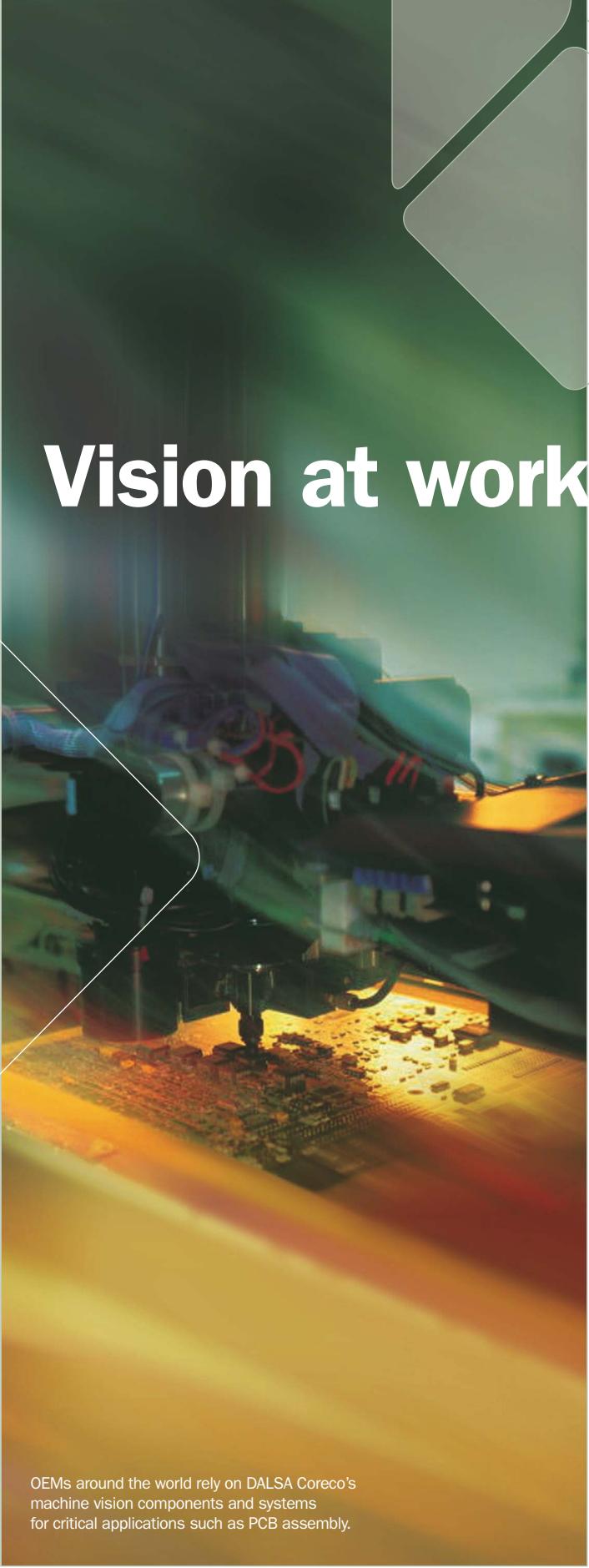


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able signal to the smallest detectable signal in a ratio, expressed in decibels (dB), provides a dynamic-range value. The ratio does not specify that an instrument can measure a specific signal. In many cases, dynamic range will equal an instrument's signal-to-noise ratio because the smallest detectable signal amounts to noise. Audio specifications may refer to an A-weighted dynamic range, which involves measurements on filtered signals between 20 Hz and 20 kHz, the range of human hearing.

Most instruments provide adjustable signal-input settings, say from $\pm 10V$ down to $\pm 10\text{ mV}$. Each setting specifies the maximum signal the instrument can work with, and each setting provides its own dynamic range. Exercise care when you determine the gain for a measurement. Say you have a 0.5 Vrms signal to measure and you can choose either a 10-V input range with a 118 dB dynamic range, or a 1-V input range with a 113 dB dynamic range. The higher dynamic range of the 10-V setting seems attractive, but do the math and you'll find that range lets you measure only down to about 12 μV . The noise floor of the instrument may hide low-amplitude harmonics and distortion produced by a device under test. On the other hand, the 1-V range with a 113 dB dynamic range lets you measure signals as low as 2 μV .

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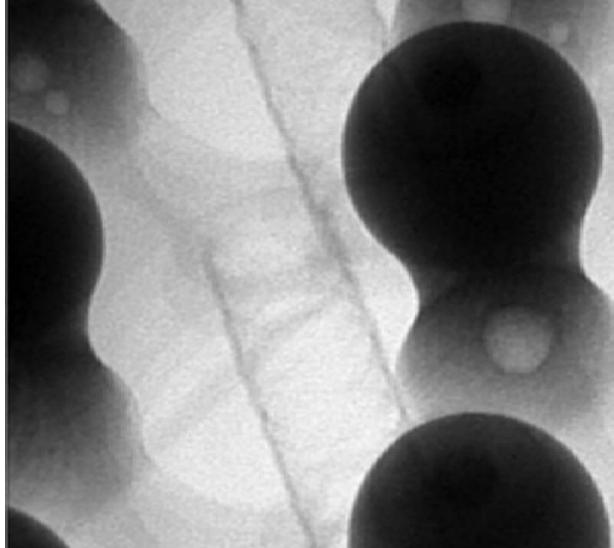
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A new technology offers a different approach to x-ray inspections.

X-RAY SYSTEMS SHARPEN IMAGES

Most test engineers understand how an x-ray inspection system can examine solder joints that are hidden under a component or are too small for other inspection techniques. But they may not know that x-ray imaging technologies perform inspections in different ways, from 2-D transmission equipment that shows everything in an x-ray beam's path to 3-D systems that can eliminate visual "interference" from components on double-sided printed-circuit boards (PCBs). Although 2-D x-ray systems remain useful, 3-D systems predominate in inspection of densely packed double-sided PCBs. (See "2-D systems remain alive and well," p. 48.)

Two well-known makers of PCB test equipment also produce 3-D x-ray inspection systems for the electronics industry. At present, Agilent Technologies' 5DX series dominates the market, but Teradyne's ClearVue system is emerging as a competitor.

Agilent's 5DX family (Figure 1), now in its fourth generation, has gone through changes that improved its repeatability and throughput, according to Glen Leinbach, an x-ray-system expert formerly with Agilent. "The basic technology should remain useful for a long time. Hundreds of systems use it," said Leinbach.

The system's laminography technology relies on a steerable x-ray beam that moves in synchronization with a rotating image detector (Figure 2). Laminography refers to the 5DX instrument's capability to image a PCB in 3-mil-thick "layers" that let test engineers view solder joints clearly on either side of a PCB.

By mathematically combining many images acquired during a scan—a complete rotation of the x-ray beam and the detector—



FIGURE 1. By continuing to refine the imaging and software capabilities of its 5DX family, Agilent Technologies has dominated the 3-D x-ray inspection market for many years.

Courtesy of Agilent Technologies.

JON TITUS, CONTRIBUTING TECHNICAL EDITOR

the system obtains an image of components free from interference from other components in the x-ray beam. In this way, a 5DX system can quickly acquire images and analyze solder-joint characteristics. Test engineers can view solder joints on the top side of the board independent of the parts on the bottom, and vice versa.

"Focus is critical in a 3-D x-ray system," explained Leinbach. A 5DX system first uses the x-ray beam to detect features on a PCB so it can align the board's x and y axes. Next, it employs a laser range finder to make a topographical "map" of the board's surface. (PCBs may have some surface distortion, such as warping.) Then, the system moves the board precisely up and down (z axis) so the x-ray beam focuses on the area of interest. The surface mapping occurs automatically, but it requires an independent scan across the board.

According to Sarah Park, business-development manager for x-ray products at Agilent Technologies, the 5DX systems can handle 0201 SMT components and can resolve solder joints spaced about 8 mils (0.2 mm) apart. When it comes to voids within solder balls or joints, the 5DX systems can detect those, too.

Software passes or fails a solder joint based on a comparison of information extracted from images and characteristics preset by test engineers. Software improvements have cut programming time considerably, and test engineers find the 5DX system easy to use, emphasized Park.

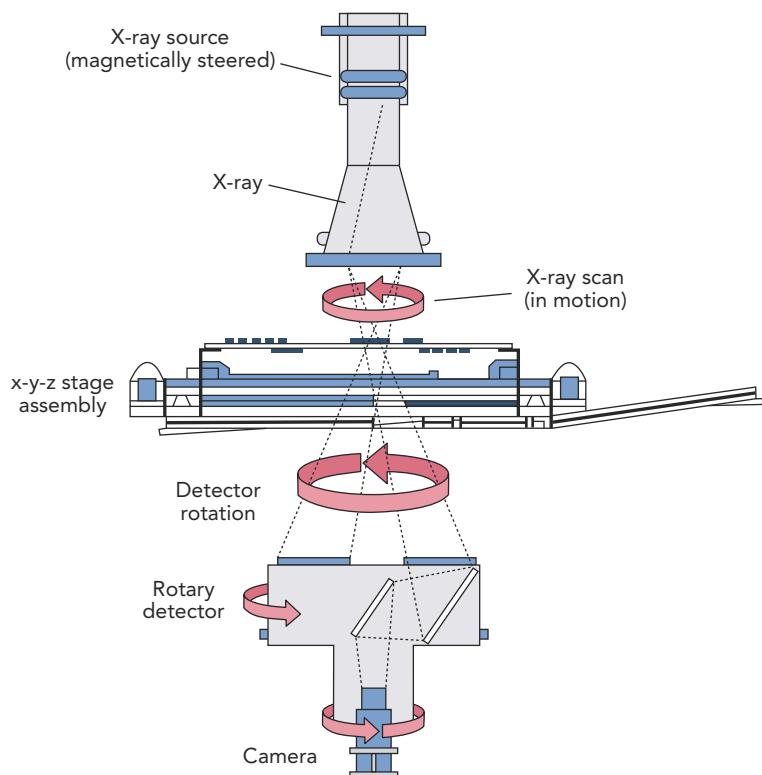


FIGURE 2. A controlled x-ray beam and a rotating detector acquire several images of an area of interest on a PCB. Software combines the images to show solder joints on only one side of a PCB.

In addition to inspecting small and hidden solder joints, an x-ray inspection system provides an analytical and diagnostic tool as PCB manufacturers make the switch to lead-free solders. Greg McIntosh, product manager for the 5DX x-ray systems at Agilent, noted customers must determine how lead-free solders will affect their production processes. "Whenever you change a process, you tend to see more defects, at least early in the changeover," said McIntosh.

"When you make a major process change, you expect certain things to happen, and they usually do," explained Leinbach. "Then, the unexpected things happen and most of them are bad. The 5DX systems help you get processes back in control and back to where you had them before the change." As they switch to lead-free solders, manufacturers will use x-ray systems to help reduce reject rates and reduce the number of products that require warranty service.

An alternative approach

Although Agilent Technologies has had the 3-D x-ray inspection field mainly to itself, Teradyne, a company that already provides 2-D x-ray equipment to the electronics industry, has now entered the market. "The laminography technique is

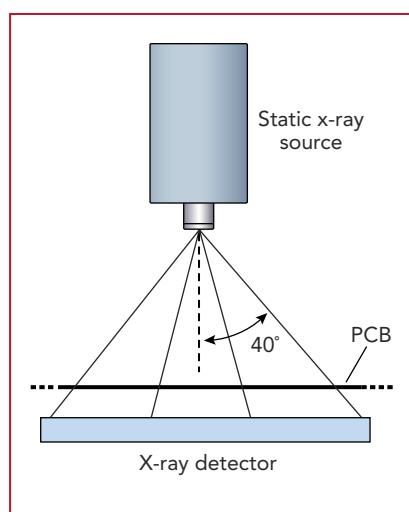


FIGURE 3. A wide-angle beam lets the ClearVue x-ray technology take off-axis images of sections of a PCB.



FIGURE 4. The Teradyne XStation MX inspection equipment provides x-ray inspection capabilities built around the ClearVue technology. Courtesy of Teradyne.

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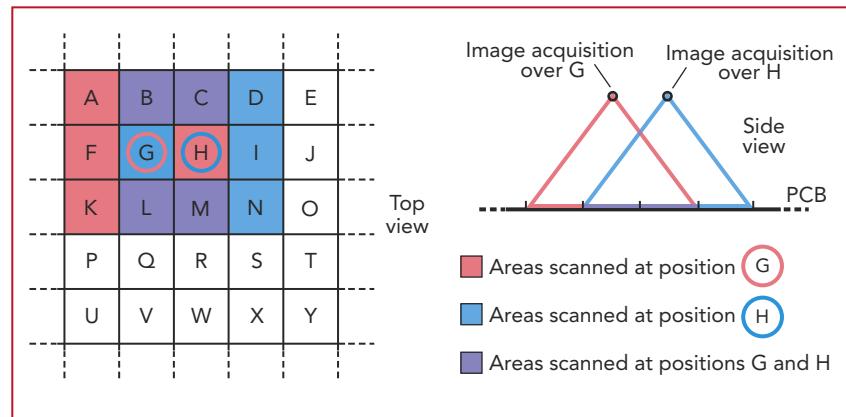


FIGURE 5. With PCB section G under the x-ray camera, the system acquires off-axis images of the red and purple sections. With PCB section H under the camera, the system acquires off-axis images of the blue areas and *different* off-axis images of the purple sections.

mechanically complex," said Paul Groome, manager of the automated x-ray inspection (AXI) products group at Teradyne. "It involves a rotating detector, a steered x-ray source, a board moving in the x-ray focal plane (z axis), and a laser topography scanner." In contrast, Teradyne's patented off-center tomosynthesis technique, called ClearVue, reconstructs 3-D slices while the x-ray source, the detector, and the PCB remain stationary. This approach to 3-D x-ray imaging inherently simplifies the inspection equipment. (The PCB moves between image acquisitions, though.)

The ClearVue technique places a wide-angle x-ray source on one side of a PCB and a large detector on the other (Figure 3). The x-ray beam passes through the board to the detector. But unlike a 2-D transmission system that views an x-ray beam straight through a PCB or a laminography system that employs a small angular beam, the ClearVue x-ray beam can expand to as many as 40°. Teradyne has just started to deliver its ClearVue technology in the XStation MX in-line automated inspection system (Figure 4).

To understand how the ClearVue technology works, imagine a PCB as a

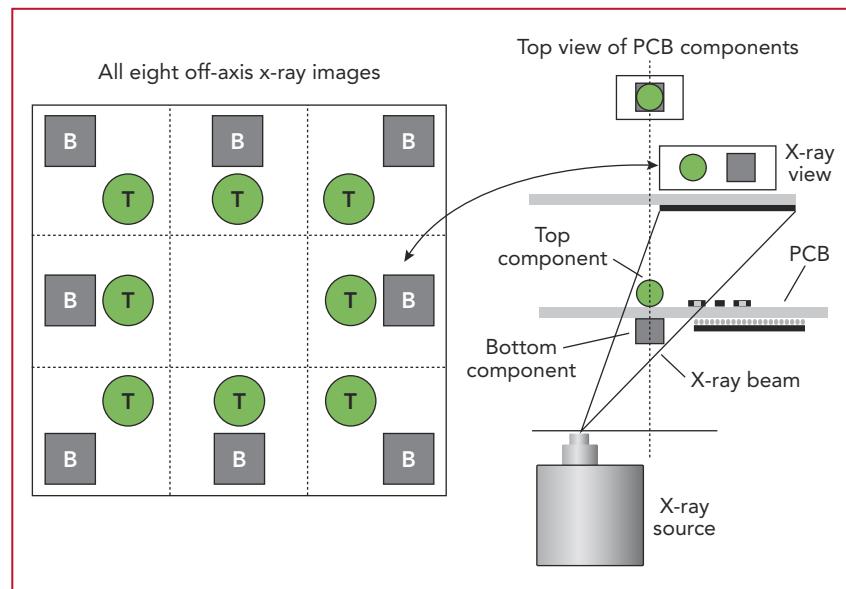
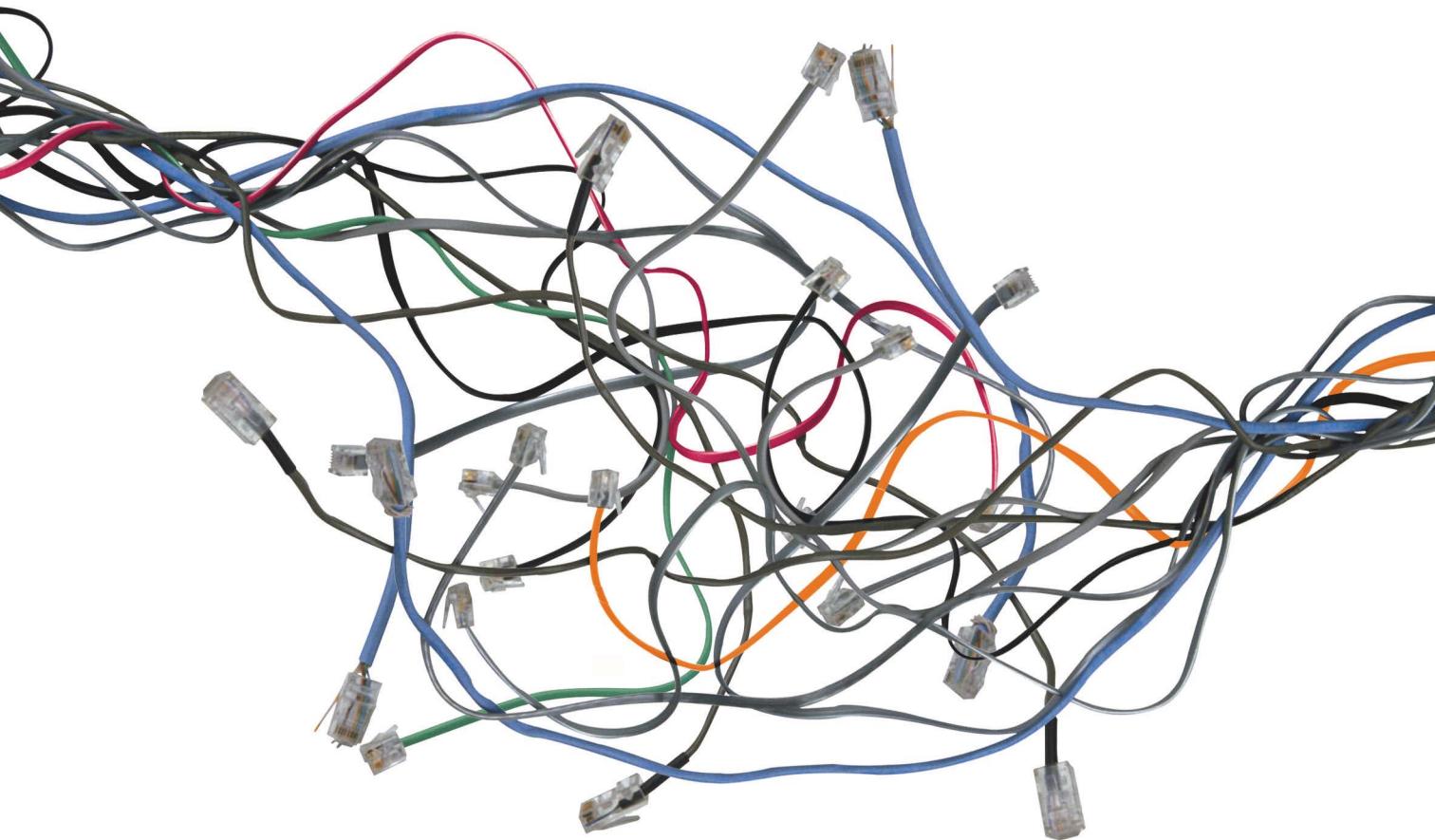


FIGURE 6. The eight off-axis x-ray images for a PCB section include all information for one section. Algorithms combine the information to let engineers selectively view components, solder joints, and other features. (Color added for emphasis.)

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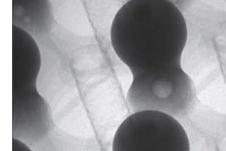
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INSPECTION

matrix of squares, or regions (**Figure 5**). Assume the x-ray system positions the PCB to place section G between the x-ray source and the detector. The system then can obtain off-axis, or angular, images of the surrounding eight sections, A, B, C, F, H, K, L, and M. When the system moves section H into the x-ray beam, it obtains off-axis images of sections B, C, D, G, I, L, M, and N. Note the system images sections B, C, L, and M a second time, but from different angles. Repositioning the PCB lets the x-ray system build up an array of eight off-axis images for each section (**Figure 6**). Then, a computer mathematically combines the off-axis tomographic information to construct an image of only the components in a selected plane.

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Because the x-ray beam passes through the PCB, each set of eight off-axis images for a PCB section contains information about components on both sides of a PCB. Thus, the ClearVue algorithms can produce images of solder joints on either side. In addition, images can portray a slice through solder joints, pads, and so on, again on either side of the PCB.

The area scanned in one image can reach 2.2x2.2 in. (56x56 mm). For that size field of view, said Teradyne's Groome, equipment can inspect 6 in²/s (31 cm²/s), about the same rate as most automated optical inspection systems. Teradyne's ClearVue technology also calculates z-axis information, so the company's 3-D x-ray equipment does not require an in-

2-D systems remain alive and well

Don Miller, president of YESTech, says companies will continue to buy and use 2-D x-ray systems for some time. In addition to inspecting PCBs on a production line, 2-D systems can provide real-time, high-resolution images of defects that 3-D systems may not resolve. "In general, hidden solder joints demand inspection by an x-ray technique, but manufacturers also may need to inspect packaged devices," stressed Miller, whose company offers 2-D x-ray systems that can resolve features as small as 1 micron.

Component densities have increased and, as a result, solder balls on IC packages such as BGAs have gotten smaller, making it more difficult to detect defects on PCBs. Thus, the high resolution of a 2-D x-ray system provides a benefit. The 2-D systems aren't perfect, though, because an x-ray image includes components on both sides of a PCB. Designers can sometimes stagger components to prevent overlap of solder pads, but small, dense PCBs may not offer that luxury.

The mandate for lead-free solders in Asia and Europe has caused apprehension among PCB manufacturers, which may lead to adoption of 2-D x-ray equipment. YESTech's Miller noted these manufacturers will use high-resolution x-ray inspections to discover the new types of soldering defects that lead-free formulations cause on their production lines.

"The lead-free alloys melt at higher temperatures, which can unduly stress ICs and components," said Miller. "So, engineers may not yet understand the types of failures and defects their processes cause. To start, PCBs and the components themselves will require the more thorough inspections that 2-D systems offer."—Jon Titus



A YESTech YTX-5000 in-line system combines automated x-ray inspection and automated optical inspection (AOI). Software provides pass/fail indications and quantitative data about solder joints.

Courtesy of YESTech.

dependent—and time-consuming—laser scan to map a PCB's surface. "Because the XStation MX systems don't rely on a lot of mechanical movements and because ClearVue technology doesn't average im-

Customers must determine how lead-free solders will affect their production processes.

ages, we can achieve false joint-defect rates below 500 joints per million solder joints inspected," said Groome.

At the 6-in./s scan rate, the x-ray detector can resolve 1 mil (0.025 mm) per pixel, which lets an XStation MX system adequately view solder joints on 0201 SMT components. Because the system can adjust the angle of the x-ray beam, it

can vary the field of view to examine packages such as flip chips and BGAs.

Unfortunately, Agilent Technologies' policies prevent its employees from commenting on competitive products, so Agilent's x-ray experts must remain mute about the ClearVue introduction. Still, Agilent's McIntosh noted, "The technology in this [Teradyne] introduction is new, so we know of no benchmark. Customers should ask for comparable data about throughput and accuracy. We haven't seen one of these systems or heard of a customer who has tested boards on it."

Test engineers will surely put any x-ray inspection equipment to good use. "Today, about 35 to 40% of all joints coming off a production line connect a BGA to a board," said Teradyne's Groome. "We have seen research that claims by 2007, an area-array package such as a BGA will hide about 50% of all joints produced. Many companies are already way above that percentage." **T&MW**

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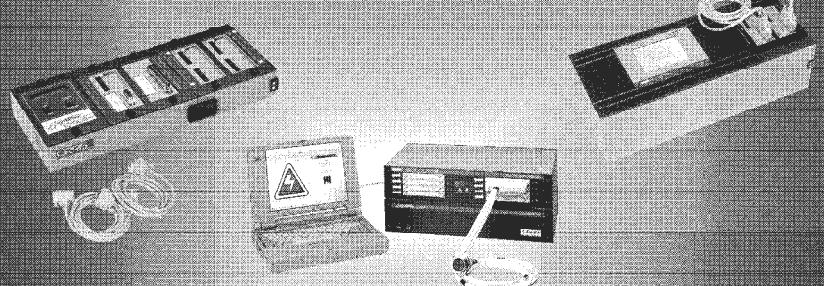
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Measurement system operates up to 3 GHz

The Integrated Measurement System (IMS) from Rohde & Schwarz combines an RF power meter, a signal source, and RF amplifiers with an optional spectrum analyzer. Covering the range of 9 kHz to 3 GHz, the IMS also includes control and switching for up to three external amplifiers to boost the signal generator's signals to required levels. Amplifiers can also boost incoming signals for emissions tests.

You can use the IMS to perform numerous measurements for EMC standards such as radiated emissions and immunity and conducted emissions and immunity. When combined with an EMI receiver, the IMS can perform radiated emissions and immunity tests. For immunity tests, the signal generator can produce signals with AM, FM, pulsed, or phase modulation. RF switches let you connect two external amplifiers to two transducers such as antennas or current probes.

Base price: \$28,500. Rohde & Schwarz, [www.rohde-schwarz.com/usa](http://rohde-schwarz.com/usa).

Serial pulse generator

Boasting a stimulus capability of up to 7 GHz, the 81141A serial pulse data generator lets you accurately characterize components for next-generation, high-speed serial buses. The instrument provides precision low-jitter signals and offers full control of data streams for stress tests. It also offers 1-GHz linear delay modulation for jitter tolerance testing and multiple data formats such as RZ, R1, and NRZ with sequencing and triggering.

Price: \$88,000. Agilent Technologies, www.agilent.com/find/7G_pulse.

Temperature humidity meter

This pocket-sized test tool measures temperature, dew point, or wet bulb from -20°C to +60°C, as well as relative humidity from 5% to 95%, ±2.5% RH. The Fluke 971 has a storage capacity of 99 data points and features an LCD with backlight and low-battery indicator. The unit runs on four AAA alkaline batteries.

Price: \$179. Fluke, www.fluke.com.



Tunable laser source

The Model 4200 laser source delivers 2000-nm/s tuning over a range of 150 nm. A low-noise version enables measurements requiring high dynamic range, such as the characterization of fiber-Bragg gratings, while a high-power version produces greater than 8 dBm (6 mW) of output power over the entire tuning range. Options such as wavelength referencing, polarization scrambling, and polarization state control, turn the Model 3200 into a fully controlled and characterized optical source.

dBm Optics, www.dbmoptics.com.

55-W enclosed switchers

Intended for battery-backup system applications, the AD55 series of high-density enclosed switching power supplies produces 55 W of output power, plus an additional battery charger output. All four models accept universal input from 85 VAC to 265 VAC and supply single and dual outputs from 13.8 VDC to 27.6 VDC. Soft-start circuitry, integral EMI filtering, power-good LED indicator, and output adjustment potentiometer are standard.

Base price: \$25 (OEM quantities). Astrodyne, www.astrodyne.com.



Power-distribution units

With over 40 models and a wide variety of factory-installed options from which to choose, the RM/RMS family of 19-in. rack-mount power-distribution units can be configured to meet any number of industrial, telecommunication, and audio power applications. Units are available with four to 10 output power sockets, as well as full line filtering and line surge protection to UL 330-V standards. Input line protection employs magnetic circuit breakers to eliminate nuisance line resets caused by momentary overload conditions. All models feature rugged steel construction and come with input AC line cords ranging from 6 ft to 15 ft.

Price: \$79 to \$125. BMF Power, www.bmfpower.com.

Sampling scope software

A software package for the TDS/CSA8000 sampling oscilloscope provides advanced jitter, noise, and BER analysis of high-speed serial data at rates from 1 Gbps to 60 Gbps. The 80SJNB software speeds the identifi-

> > > > > >

cation of the underlying causes of both horizontal and vertical eye closure through separation of jitter and noise. With its insight into the constituent components of both jitter and noise, 80SJNB provides complete BER extrapolation and eye contour analysis.

Tektronix, www.tek.com.

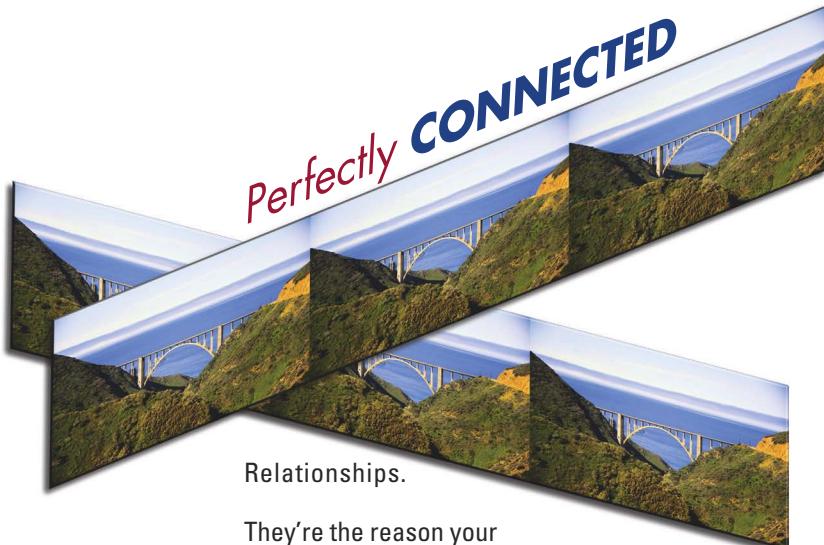
Signal integrity analyzers

To ensure the accuracy of critical measurements, Wavecrest has increased the oscilloscope bandwidth of its entire family of signal integrity analyzers to 13 GHz. The combination of the bandwidth improvement and robust jitter analysis tools included within the SIA family's

GigaView software provides a means for measuring signal integrity for standards such as PCI Express 2 (5 Gbps), SATAII (3 Gbps), 4X Fibre Channel (4.25 Gbps), and XAUI (3.125 Gbps).

The bandwidth enhancement is available free of charge as a GigaView 1.5 software upgrade for existing SIA 3100, 3300, 3400, and 3600 users. It is included as standard software on new purchases.

Wavecrest, www.wavecrest.com.



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All three models in the 300 series of digital multimeters are equipped with built-in noncontact AC voltage detection to enable you to check for voltage prior to attaching the meter's test leads to the device under test. Each unit measures DC/AC voltage to within 0.5% basic accuracy, along with DC/AC current and resistance. Additionally, the EX310, EX320, and EX330 perform diode testing, have an audible beeper for continuity testing, and include a low-battery indicator. The auto-ranging EX330 features a 4000-count display and measures temperature, capacitance, frequency, and duty cycle. The auto-ranging EX320 and manual-ranging EX310 have 2000-count displays.

Extech Instruments, www.extech.com.

USB digital I/O module

Joining the ECON series of mini-instruments, the DT9817-H provides high-drive digital I/O capability for the USB



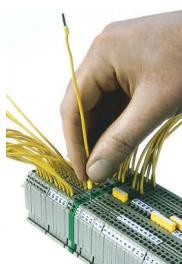
2.0 bus. The DT9817-H furnishes 28 programmable digital I/O lines and can sink 64 mA or source 15 mA at standard logic levels. Simply install the supplied GO! software, connect your signals to the screw terminals of the module, and plug the module into the USB port of your computer. For more advanced applications, the module also ships with extensive software tools, including DTx-EZ for Visual Basic or Visual C++, DT-LV

Link for LabView, and an evaluation copy of DT Measure Foundry.

Price: \$179. *Data Translation*, www.datatranslation.com.

Spring-connection terminal blocks

Using a stainless-steel leaf spring clamp connection, the FRK series of terminal blocks reduces wiring time by as much as 80% when compared



to screw clamp terminations. The system, which accepts solid or stranded wire with a ferrule, requires no tools and allows fingertip wire installation that needs minimal insertion force. Spring pressure ensures firm wire retention. The FRK series comprises feed-through and ground terminal blocks in 2-clamp, 3-clamp, and 4-clamp configurations. Block widths of 4 mm, 5 mm, and 6 mm accommodate wire sizes up to 16 AWG, 12 AWG, and 10 AWG, respectively. Feed-through terminals are rated at 600 V and carry up to 32 A.

Conta-Clip, www.contaclipinc.com.

Megohmmeter

Small enough to fit in your pocket, the Ohm-Stat RT-500 measures surface resistivity using parallel electrodes and concentric rings. It also tests resistance to ground (RTG), resistance between two points (RTT), and volume resistance using two 5-lb, 2.5-in. disk probes. Press the button on the front of the meter and it automatically measures either 10 V or 100 V, depending on the resistance of the material. LED display color indicates range.

Price: \$450. *Static Solutions*, www.staticsolutions.com.

Graphical programming software

To address a variety of skill levels, Measurement Computing is offering four versions of its DASYLab graphical programming software for designing complex data-acquisition applications using a simple GUI. The

software offers over 90 data-acquisition, control, processing, and display functions across 10 categories, or modules, including inputs/outputs, trigger, control, display, and signal analysis. DASYLab Full comes with all 10 standard modules, 200 layout options, and a sequencer. The Pro version adds an analysis toolkit bundle.

Prices: DASYLab Lite—\$495; Basic—\$1099; Full—\$1499; and Pro—\$1999. *Measurement Computing*, www.mccdaq.com.

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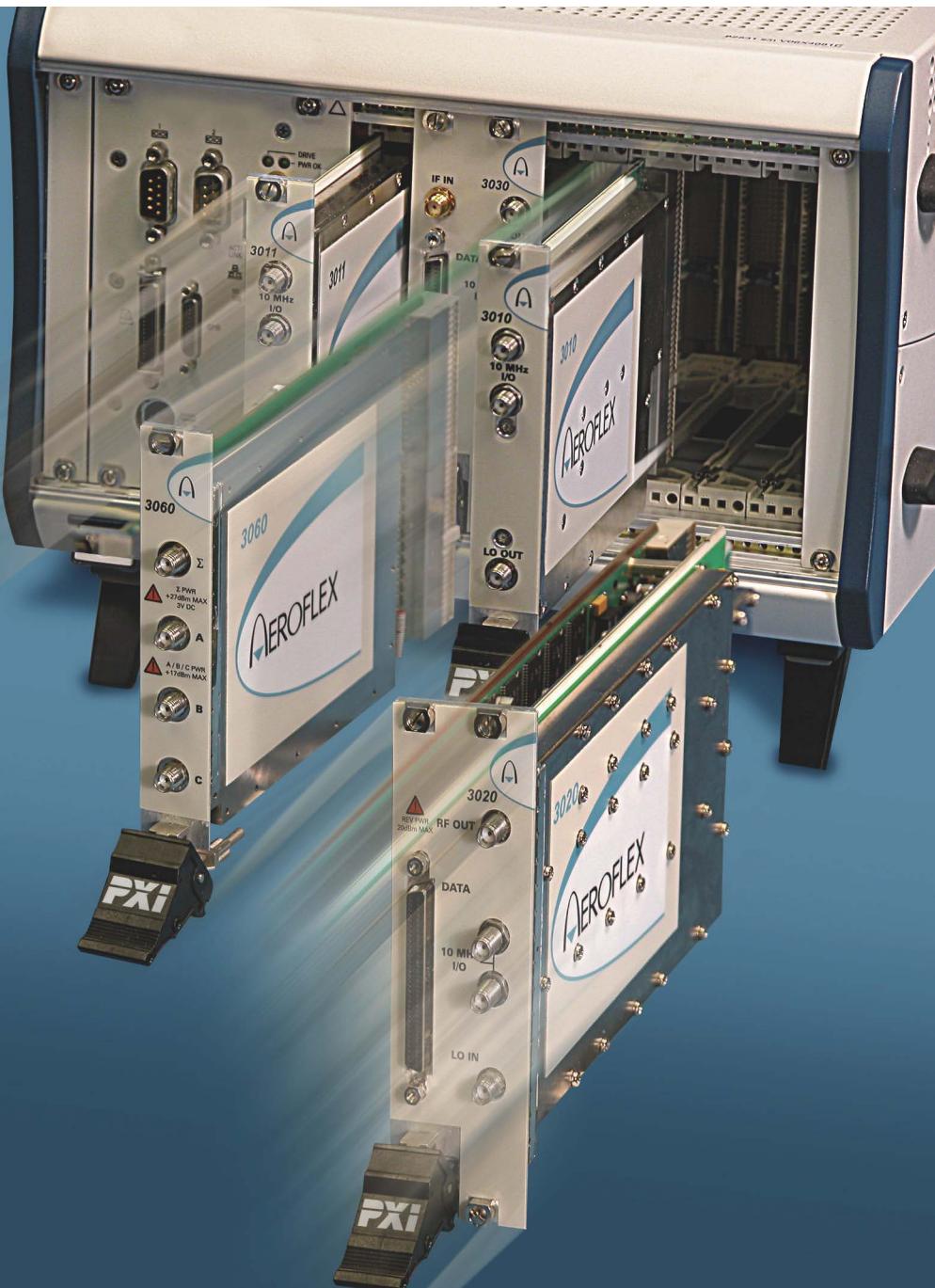
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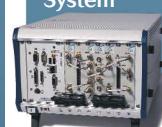
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UWB wireless implementations get boosts

Rick Nelson, Chief Editor

Two wireless communications implementations related to ultra wideband (UWB) and the PC's USB (Universal Serial Bus) have received significant boosts within the last two months with respect to standards efforts and the debut of a protocol tester that supports both. In addition, a UWB reference design and a USB peripheral developer kit have emerged to give further impetus to the development of products embodying the respective standards.

The WiMedia Alliance (www.wimedia.org) announced on August 15 that it is now working with Ecma International (www.ecma-international.org), the organization known for its development of DVD-interchange, scripting-language, consumer-electronics, and other standards. The goal is to establish the WiMedia multiband orthogonal frequency-division multiplexing (MB-OFDM) UWB radio platform as the global UWB standard and to ensure that the UWB industry does not become fragmented by independent regional standards or proprietary implementations that prevent global interoperability, an environment that the WiMedia Alliance reports could delay the worldwide market adoption

of UWB products. The WiMedia implementation targets low-cost, low-power demands and data rates to 480 Mbps and beyond.

"We are very pleased to be working with Ecma, who make it possible to quickly complete the process of establishing a recognized international standard by the end of this year, which corresponds to UWB product launches," said WiMedia Alliance president Stephen R. Wood in a prepared statement.

Certified Wireless USB, which is based on WiMedia's MAC and PHY architecture and promulgated by the USB Implementers Forum (USB-IF; www.usb.org), will benefit from two announcements made by Intel at its Intel Developer Forum (August 24, 2005, San Francisco, CA; www.intel.com/idf).

First, Intel is developing a Wireless Host Controller Interface (WHCI) specification with support from companies including Microsoft, NEC, Philips, and Texas Instruments; the goal is a standardized method of hardware-software communication that will lead to delivery of interoperable products in 2006. Second, Intel is opening an interoperability lab that will provide an environment where companies can perform initial tests on Certified Wireless USB and WiMedia implementations before submitting products to the USB-IF.

Product support

The new instrumentation comes from Ellisys, a Geneva, Switzerland, supplier of USB test products. Its new Wireless USB Explorer 300 protocol analyzer supports UWB specifi-



The Wireless USB Explorer 300 can record and decode WiMedia and Certified Wireless USB protocols. Courtesy of Ellisys.

cations from the WiMedia Alliance and the Certified Wireless USB standard. The instrument is designed to smooth firmware and driver development, prevent interoperability problems, verify data encryption, optimize performance, tune power management, and improve communication reliability.

The Wireless USB Explorer 300 can record and decode WiMedia UWB and Certified Wireless USB protocols from different perspectives: It can record traffic exchanged between devices over the air through its external omnidirectional antenna, and it can capture traffic between MAC and PHY layers from boards under development.

In further support of WiMedia and Certified Wireless USB, chipset maker Wisair has announced a UWB host-dongle reference design—a 23x69-mm board that includes an onboard antenna and that plugs into any USB 2.0 host port. In addition, Intel has released a peripheral development kit (PDK) for Certified Wireless USB; the \$5000 PDK consists of a PCI add-in card and some debug tools. □

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EDITOR'S NOTE

Prepare for VoIP

Richard A. Quinnell, Technical Editor

A revolution is brewing in communications. It has been a long time simmering—the technology was developed years ago—but it now appears to be on the brink of boiling over. The revolution is a switch from traditional telephony to Voice over Internet Protocol (VoIP).

VoIP has been making inroads into both enterprise telephone networks and cellular telephony as a way of combining data and voice communications in the same system. Added to that is a growing interest in video communications, making VoIP part of a triple-play communications system.

Turning over a company's essential communications to this technology represents a huge risk for early adopters as the technology settles into place. Even mainstream adopters will risk a communications shutdown if the new systems have problems. The way to minimize those risks is to test, retest, and test again the components and the infrastructure for a wide variety of factors, including quality of service, load tolerance, and interactions of the voice, data, and video communications streams.

Such testing will have to handle standard networks as well as telephony and wireless systems carrying digital voice and video. Systems will need to be tested for both function and capacity with tests monitoring quality of service (QoS) in the presence of massive data transfers. Testing will be needed before installation and for ongoing maintenance.

A revolution is brewing, and with it will come unprecedented opportunity for communications test engineers. Are you prepared? □

Contact Richard A. Quinnell at richquinnell@att.net.



PRODUCTS

Instrumentation bridges debut

North Hills has announced a line of instrumentation bridges that measure the transverse or differential signal resulting from the application of a longitudinal or common-mode signal to a balanced network. "The LBB series uses a patented magnetic circuit to achieve an essentially frequency-independent inherent balance that exceeds 60 dB at 300 MHz," said Richard Schwarz, North Hills GM. He explained that the new bridges, used in conjunction with 50- Ω network analyzers, support measurement of longitudinal conversion loss (the ratio of the differential response voltage to the applied common-mode voltage) of twisted pair networks. *North Hills*, www.northhills-sp.com.

800-MHz generator debuts

Signal Forge has released a digitally synthesized signal generator with an 800-MHz range, usable to 1 GHz, for



less than \$1000. The Signal Forge 800 (SF800) features a dedicated digital output with programmable voltage levels for testing digital systems and integrated circuits. It also provides an AC coupled output and a differential output for testing wireless devices.

Peleton releases multi-wavelength laser

Peleton has released a 96-channel laser source that generates light at 96 discrete wavelengths with channel spacing of 50 GHz. Wavelength range is 1527.60 nm to 1565.50 nm. Typical output power is 3.5 mW/channel.

You can use the TM3050C to test optical subsystems such as amplifiers, optical channel monitors, and optical switches. It also performs DWDM system verification, dynamic network simulations, multi-wavelength sensing applications, and optically steered phased arrays. *Peleton*, www.peleton.com.

The SF800, which measures 8.5x5.5x1.5 in., produces both sine waves and square waves from 1 kHz to 1 GHz in 1-Hz increments. Applications include characterizing narrow-band communication systems as well as the IF and RF section of receivers and subsystems. *Signal Forge*, www.signalforge.com.

Service monitor reaches 2.7 GHz

The IFR 3902, based on Aeroflex's 1-GHz IFR 3901, expands the operating range of the service monitor to 2.7 GHz for both generating and receiving analog and digital RF signals. New firmware for the IFR 3902 and the IFR 3901 supports analog duplex test capabilities as a standard feature. The units also support an optional Site Monitoring Application, which allows a system engineer to set up the unit for a particular channel or frequency and then find the effective sensitivity level. *Aeroflex*, www.aeroflex.com.

Test set supports VoIP

The CoVALT instrument from Consultronics can test VoIP that is delivered using ADSL, ADSL2, ADSL2+, and Reach Extended (RE) ADSL Annex L. Once a DSL connection is established, the installer can place or receive a VoIP call over the CoVALT's integral telephone style microphone and speaker. The \$2480 CoVALT can also connect directly to the RJ-45 Ethernet jack inside the customer premises to test a router-based VoIP port. *Consultronics*, www.consultronics.com.

Double-barreled WiFi test

Richard A Quinnell, Contributing Technical Editor

Wireless networking based on the IEEE 802.11 standards is poised for substantial growth in both the numbers of units and the range of their applications. The mobility inherent in wireless networks, however, creates interactions between the physical and the protocol layers that—compared with wired networks—greatly increase the complexity and number of tests necessary to verify a design. Fortunately, tools are becoming available to streamline the process.

The 802.11a/b/g standards, collectively known as WiFi (Wireless Fidelity), have engendered a large and growing market among home users, who are finding wireless a simpler alternative to Ethernet for sharing resources such as printers and broadband connections in their homes. In addition, business users that need mobile-computing capability are adopting the technology in droves. Public WLANs (wireless local-area networks), or “hot spots,” are also increasing in popularity with both business and home users. The result: worldwide WiFi-equipment revenues of \$737.6 million in the first quarter of 2005 alone, a 15% increase over the first quarter of 2004, according to market-research company In-Stat.

Although the adoption of WiFi in homes and businesses for computer access is still rising, new markets for the technology are poised to emerge. In-Stat is tracking promising applications, such as VoWLAN (voice over WLAN), the use of WiFi as a means of consumer-electronics connectivity, and the combination of VoWLAN with cellular telephones. Each represents a market that could match or exceed that of computer access.

This article previously appeared in the September 1, 2005, issue of our sister publication, *EDN*. www.edn.com.

Testing a WiFi design requires a combination of RF- and data-level test equipment that designers must use together to fully exercise the protocols. Courtesy of Agilent Technologies.



The rise of these major markets could result in many designers facing for the first time the challenges of WLAN test. The challenges are significant, and designers' experience with more traditional cabled networking is an insufficient background for meeting them. WLAN is more than traditional networking with a radio-based physical-layer interface.

Complex protocols complicate testing

For one thing, the protocols are more complex, says Thomas Alexander, PhD, CTO at VeriWave. He notes that many extra features in WLAN protocols address three aspects of wireless LANs that cabled networks lack: dynamic configuration, a spatial nature, and mobility. These aspects add to the complexity of wireless testing. The dynamic-configuration aspect of WiFi allows endpoint stations to query APs (access points) to gain network access and has APs announce the services they support. Although cabled networking has comparable functions, they are typically present in higher layer protocols. WiFi implements them at the MAC (media-access-control) layer. WiFi stations must also use “association” to determine which AP to use when several are available, and the APs must use “authentication” to determine whether the station is a valid user before granting access. Physically secure cabled connections need no authentica-

tion. A radio connection could come from someone parked down the block trying to get free Internet access.

The spatial nature of WiFi creates situations, such as “hidden nodes,” that you don’t find in cabled networks. In such situations, two stations can be in range of an AP yet not in range of each other. As a result, the two can repeatedly clash when trying to send messages to the AP because neither can detect the collision. Similarly, in cabled networks, careful design and installation can control the noise levels in the physical layer, and switches can segment the network into manageable groups. Designers of wireless-network devices, however, cannot assume a controlled environment. WiFi shares its frequency band with Bluetooth, portable phones, and microwave ovens, among other RF sources. Designers also cannot control the number of stations that may be actively attempting to reach an AP. The protocols must allow the network to simply adapt to the environment it finds.

The mobility aspect of WiFi also imposes functions on equipment and protocols that cabled networks don’t need. One added function is that battery-operated stations may need power management to optimize power dissipation, such as by turning down transmitting power when close to an AP to save energy. One added protocol function is the ability to dy-

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namically switch a station between APs during a transmission, similar in nature to cell-phone roaming. Another added protocol function is rate adaptation, the ability to adjust the signaling data rate based on the received signal power to optimize the overall channel performance.

Layers not fully separable

Another complication arises beyond the more complex protocols, however. With cabled networks, engineers can independently test system layers and then simply combine the tested components to assemble a working system. Following the traditional network-testing model, testing of wireless-networking-device designs would have two major tasks. One task would be for digital and software engineers to evaluate the device from the network side by using protocol and logic analyzers. The other component would have RF engineers evaluate the radio section using vector-signal and spectrum analyzers along with signal generators, oscilloscopes, and other RF equipment.

But, the old adage "the whole is greater than the sum of its parts" applies in spades to testing WiFi product designs. The physical and protocol layers need not only independent testing, but also simultaneous testing to verify the proper operation of higher layers. This situation leads to a requirement for many pieces of equipment, both RF and digital, working in concert to create the necessary test conditions and measure the results.

Fortunately, RF-test-equipment vendors have been working to consolidate and automate some of the necessary equipment, and many such

products emerged in mid-2004 to late 2004. Agilent Technologies created the N4010A wireless-connectivity test set, which uses software modules to implement signal- and vector-analysis functions, as well as signal generation, and to form a more self-contained RF-test package. Similarly, Anritsu offers software for its spectrum analyzers to combine several WLAN RF-test abilities in one instrument. LitePoint has IQView for testing WiFi transmitter and receiver functions. The company also offers IQWave software for creating custom signal waveforms with the instru-

ment. The difficulty of WiFi testing emerges most strongly in this area. To provide repeatable tests, the DUT (device under test) needs a controlled stimulus. This requirement means at least testing the unit in a shielded enclosure to isolate the unit from

stray signals. In addition, the stimulus signals must have controllable strengths, which involves the use of programmable attenuation. In addition, to simulate a full network configuration, multiple stimulus signals from independent sources must be present.

Protocol test

Unfortunately, most of the RF-test instruments available directly stimulate the DUT with a single signal. Testing the device in a multisignal environment has required the use of many instruments. Coordinating the signals from these multiple instruments to create repeatable test conditions using a home-brewed test setup has been difficult at best. The test setup requires either using a complicated cabling scheme with manual calibration of each source to feed the DUT in a shielded enclosure or placing the entire test configuration in a Faraday cage, a metallic enclosure that prevents the entry or escape of an EM field, to gain repeatability.

Having covered the testing of the physical-layer components, it would seem that testing the higher layers would simply require digital pattern generators and protocol analyzers. But WiFi's complex protocols must

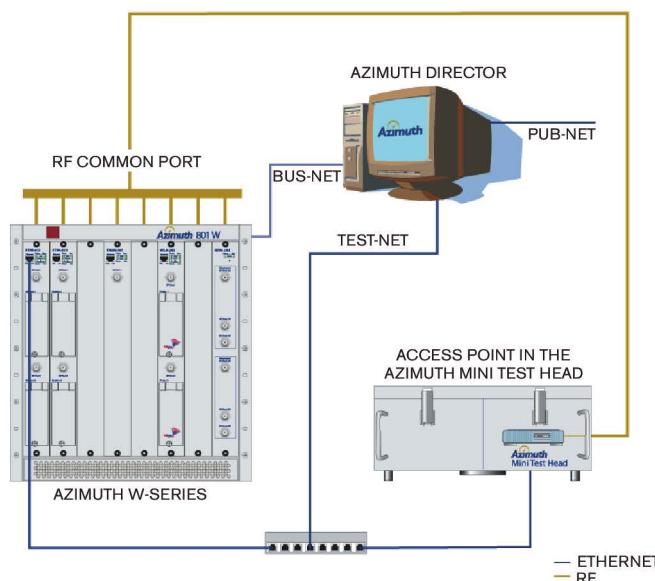


Fig. 1 To emulate an entire WiFi network, the Azimuth Systems W-series test equipment provides a mix of WiFi signals under program control to the device under test.

ments to test response to impaired waveforms. Most recently, National Instruments has entered the market with a PXI-based instrument package with its LabView development software and a software package from SeaSolve Software that runs physical-layer-compliance tests on WiFi-radio units.

Having covered the testing of the physical-layer components, it would seem that testing the higher layers would simply require digital pattern generators and protocol analyzers. But WiFi's complex protocols must

movement of the DUT or the stimulus signals to fully exercise the unit. "The whole idea behind WiFi is mobility," says Ray Cronin, CEO of Azimuth Systems. "You have to have a system that will test the effect of mobility on the quality of service."

Providing the means to generate multiple controlled stimulus signals, along with simulating the effects of mobility by using programmable attenuation, has been the focus of companies such as Azimuth, Ixia, and VeriWave. All of these companies have products that provide protocol analysis as well as allow the coordinated generation of multiple test signals for evaluating WLAN devices under a wide range of conditions.

The companies have different approaches to the testing, however. The Azimuth W-series test platform provides a shielded enclosure for the DUT, feeding it controlled signals

through a cable system (Figure 1). The test signals come from a bank of generator modules under the common control of a computer system that specifies the function of each module, coordinates signal activity, and manages the combination of the RF outputs using programmable attenuators. This approach allows the system to mimic a variety of traffic patterns and signal conditions, including roaming, in a repeatable configuration without the need for a shielded room.

The Ixia IxWLAN and VeriWave WaveTest systems allow both a cabled and an open-air approach. The systems feature synchronized control of numerous test-stimulus devices to generate the network signals and offer control of both the transmitting power and receiver thresholds of the test-stimulus devices to handle spatial relationships. The systems can work in a cabled configuration, in a Far-

aday cage, or in an open-air field environment. The VeriWave system can also capture signals in the field for later playback under laboratory conditions.

A key attribute of all three systems is their scalability. They allow the creation of test setups that can mimic dozens of access points with hundreds of stations, all under automated control. This approach allows for testing of designs against the crowded conditions users are likely to find in actual installations as well as the measurement of system performance under such conditions. The tests can thus help system administrators plan their installations to optimize throughput.

Another key attribute of these systems is the level of automation they provide. Development teams can outfit these systems with vendor-provided software that implements a complete compliance-test suite using the sys-

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Communications

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tem. Running these test suites does not provide design certification but does assure development teams that their designs will achieve certification.

Such protocol test systems help round out the testing of WiFi devices by addressing network issues during the test. They do not, however, provide measurement of the RF parameters, although the WaveTest system can generate triggering signals to RF-test equipment to coordinate such measurements. Test engineers must test the RF portion and the data portions separately. WiFi testing may be consolidating its tools, but some two-step procedures still occur.

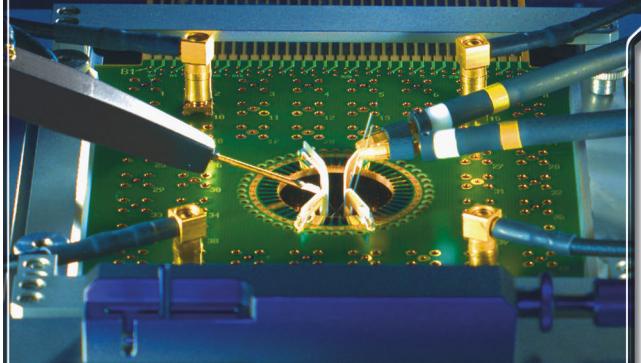
Test systems lag

That two-step dance is likely to continue for some time. As Azimuth's Cronin points out, "A new technology evolves ahead of the test technology to support it." In the case of WiFi, the technology is still evolving. In addition to versions a, b, and g, new versions of the 802.11 standard are in development. The 802.11q standard, for instance, allows the mapping of virtual LANs onto the wireless network. The 802.11i version adds new security protocols to the network to bolster the privacy of wireless connections. Another trend adds voice to the wireless networks, requiring controlled quality of service and timing.

To meet the ever-changing needs of WiFi designs is WiFi testing's ultimate challenge. Traditional hard-wired products are too slow to adapt to the rapidly changing technology. Today's wireless test equipment must be adaptable through software if there is to be any hope of keeping pace.

National Instruments is taking the programmability approach in its RF-test system, according to modular-instrument product manager Darcy Dement. "As technology evolves, so must the test," says Dement. "When the equipment is software-driven, it lets designers keep their tools in line with the changing standards. Having an open architecture, such as LabView, also allows designers to get into the test parameters to customize them for their unique needs." Azimuth's Cronin agrees that programmability is key to test's keeping pace with changing standards. "Without the programmability built into tools such as ours, changes in the standards would put the onus on the developers to create their own ad hoc tools," says Cronin.

With complete system-test tools now available, automated RF testing, and tool programmability providing a path for tracking changes in the standards, developers are in a good position to embrace WiFi in their next designs. The test tools to exercise and validate designs are becoming more available—whether for game systems to talk with broadband connections, music players to send data to sound systems, or cell phones to switch from WANs to LANs. The presence of these standardized test tools can mean only more innovation and faster growth in wireless networking with less designer frustration. □



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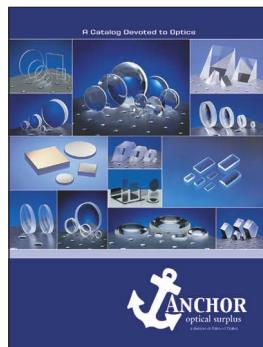
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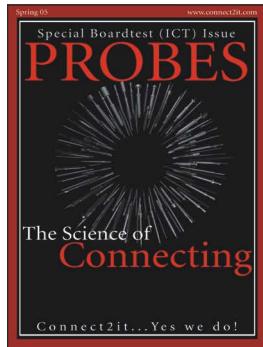
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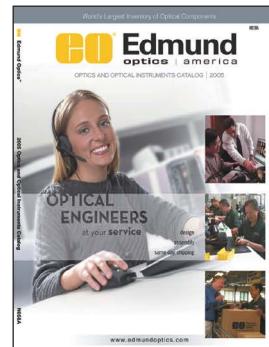
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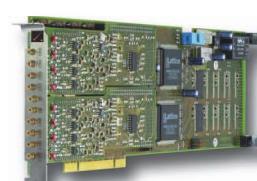
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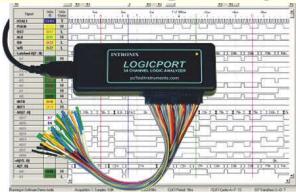


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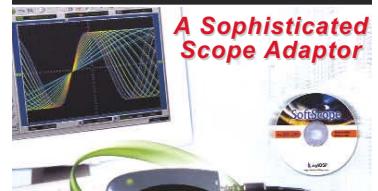
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GLENN WOPPMAN

President, CEO, and
Chairman of the Board
Asset InterTech
Richardson, TX

Glenn Woppman has been closely involved with boundary scan since the late 1980s. Prior to being named president and CEO in 1995, when Asset InterTech became an independent company, he was product manager for the Asset business unit within TI, where he was responsible for all business functions relating to Asset, including sales, marketing, R&D, and finance. He holds an MBA from SMU and a BSIE from the University of South Florida.

► Woppman elaborates on relationships in the online version of this article, which includes more Q&A on boundary-scan challenges and the technology's evolution and future:

www.tmworld.com/archives

Relationships key to boundary-scan success

Asset InterTech began as a business unit within Texas Instruments during the early days of boundary scan, where it was responsible for developing the technology as well as the market. In 1995, the company was spun off from TI and is now celebrating its 10th anniversary.

T&MW: Why did Asset InterTech separate from TI?

Woppman: First, we needed to have relationships with other semiconductor companies, and being a business unit within TI was going to make that difficult. Second, TI went through a self-assessment and decided to become focused on DSP and analog, so it was good timing for both of us.

T&MW: Could you summarize Asset's offerings?

Woppman: Our lead product is our ScanWorks boundary-scan development environment for developing structural tests and for device programming. Complementing that, we have a services group that serves customers new to the technology who might rather have an expert develop their first boundary-scan test program. Once they are up to speed, they often move into using ScanWorks themselves.

T&MW: What differentiates Asset from other boundary-scan companies?

Woppman: Our development environment. Large, leading-edge companies pushing the envelope of technology want lots of capabilities and a rich feature set, and we provide that. But at smaller companies, you have one guy who's the board designer, but he's also doing some embedded software design, and oh, by the way, he needs to make sure he can debug and test his board. For him, a feature-rich environment is nice, but his key requirement is usability. He needs to be able to use a tool in January, put it down, and come back in July and quickly get back up to speed. We help this customer by including ease-of-use features like an intuitive GUI and our ScanWorks Assistant, and by making support instantly available over the Web. For instance,

right within our user interface, he can get a 5-min video refresher on how to do an interconnect test. We track the use of these features, and we've seen activity surge as we've added more capabilities

T&MW: What's the biggest challenge limiting acceptance of boundary scan?

Woppman: The big challenge we see is really at the board-level design-for-test area. If you look at the chip-development environment, the EDA vendors—Mentor, Cadence, Logic Vision, and now even Magma—all have a pretty rich set of robust, automated design-for-test tools that make it easy for designers to insert testability. But if you look at the printed-circuit-board world, the market leaders who develop schematic capture and layout tools—Mentor and Cadence dominate that market—the test tools they have don't go much beyond inserting test points. So, sometimes we'll get a board, analyze it, and find some problems—for example, the scan chain isn't properly connected to the six BGAs on the board. We can help develop workarounds for such problems, but the process would be smoother if the issues had been identified earlier.

T&MW: What are the prospects for 1149.6 AC boundary scan?

Woppman: Encouraging. LogicVision has done work on dot-6 synthesis tools, and semiconductor makers are bringing dot-6 devices to market. We added optional dot-6 support to ScanWorks about a year ago, and most of our major accounts have purchased it.

T&MW: What makes Asset InterTech unique?

Woppman: In one word, relationships. T&MW

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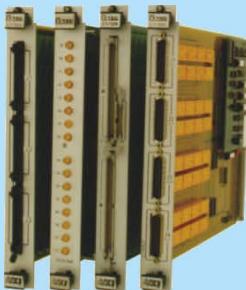
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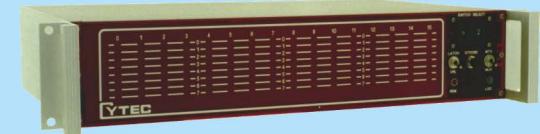
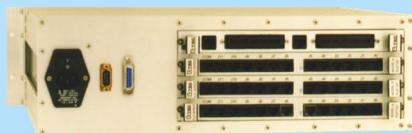
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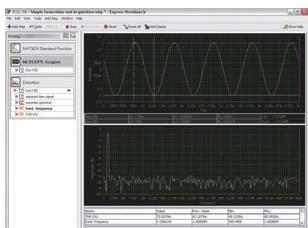


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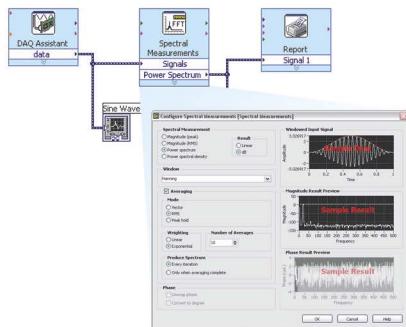
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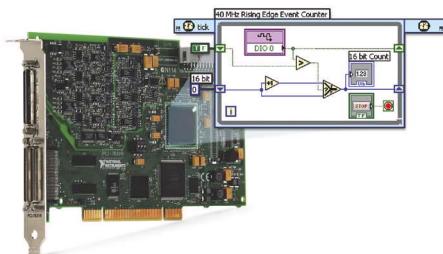
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